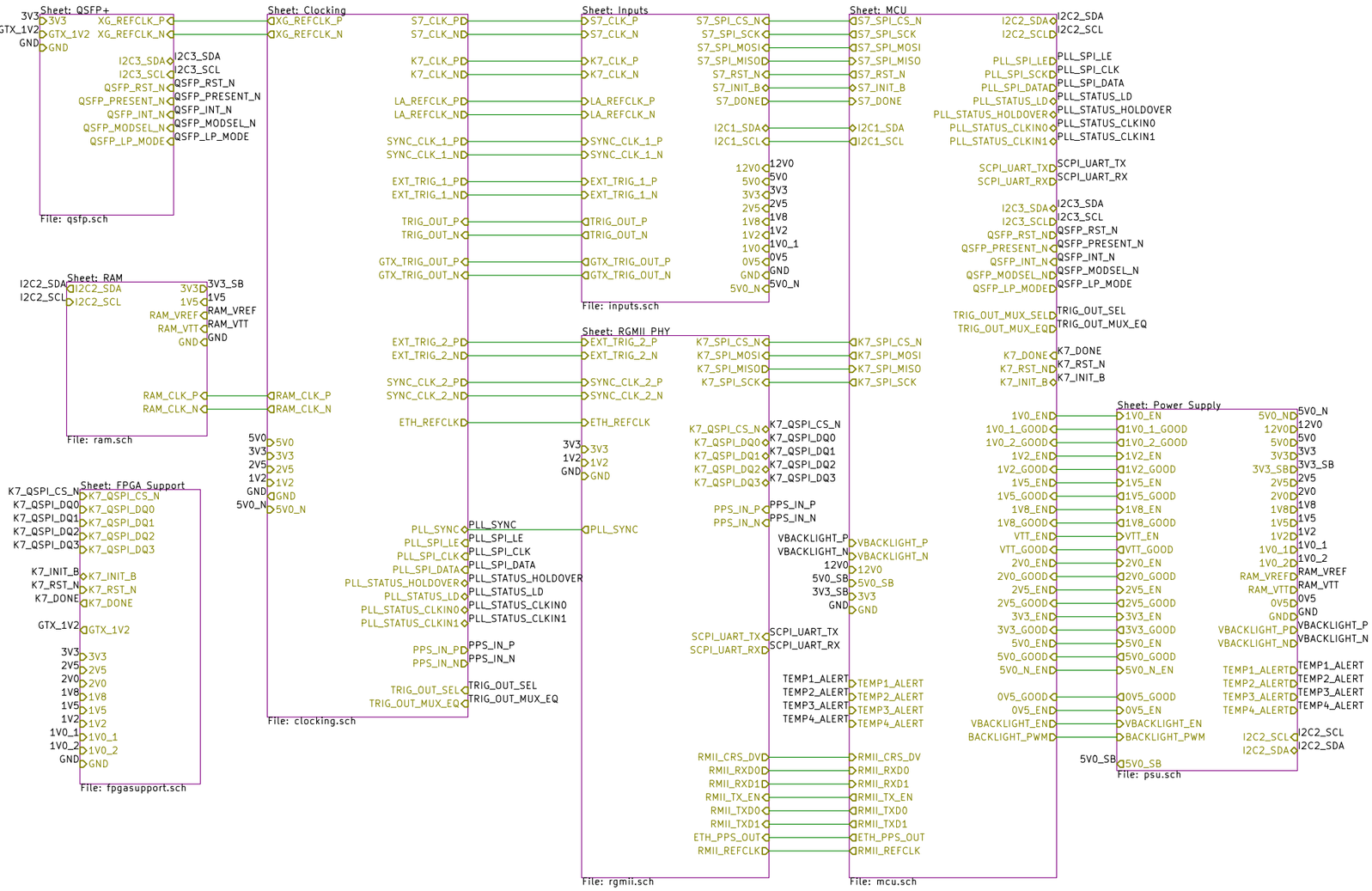

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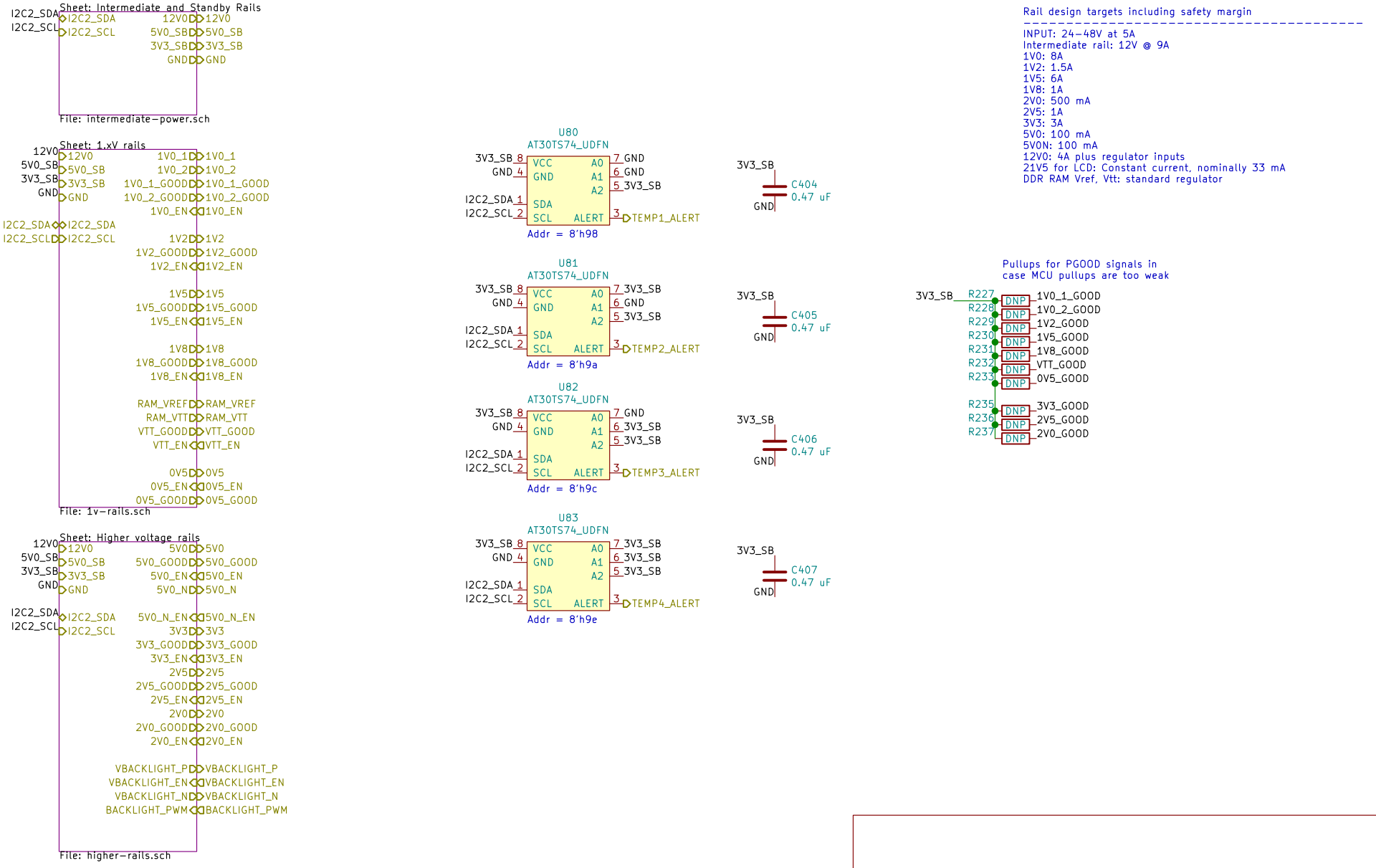
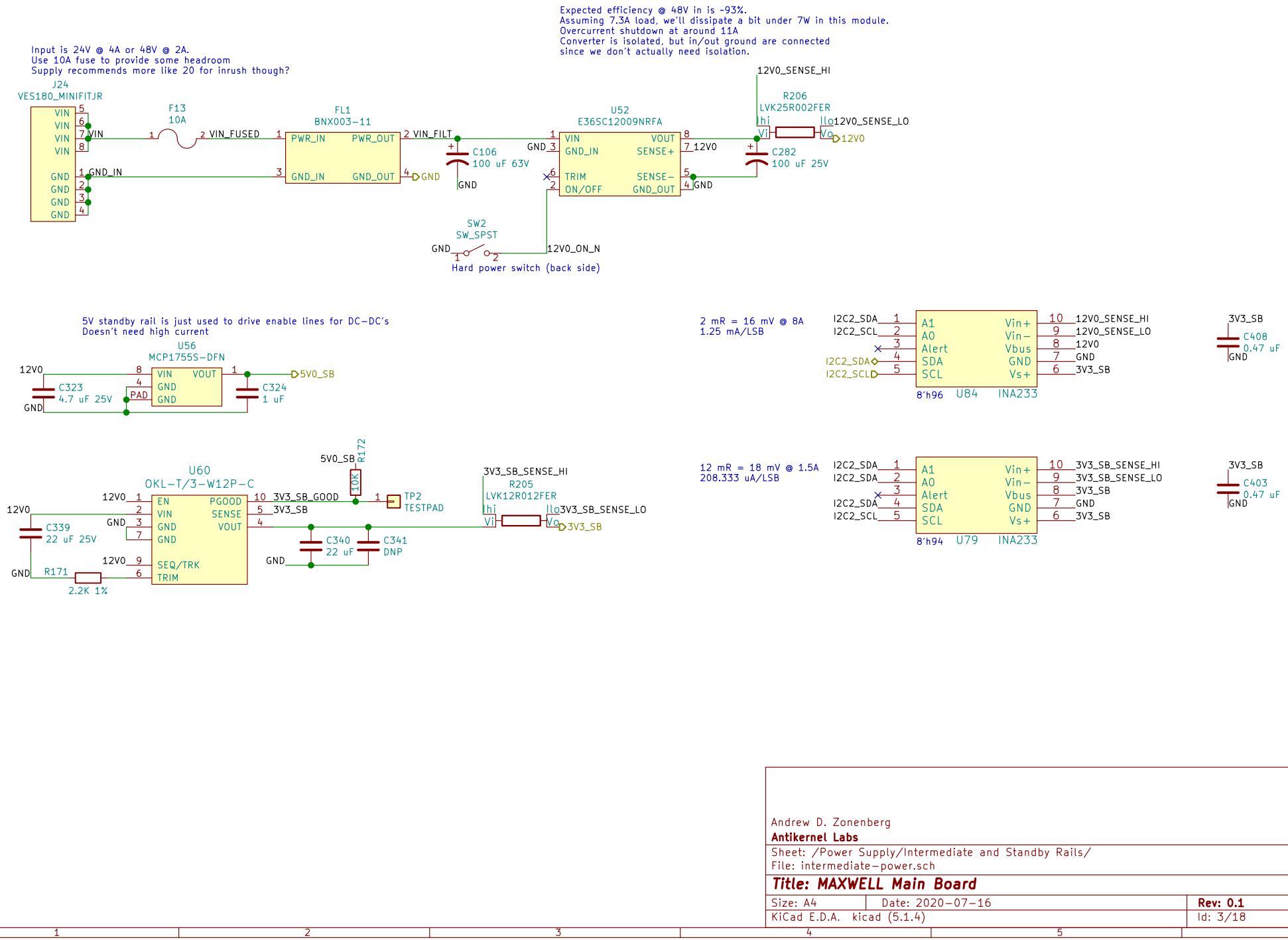
Sheet: /
File: maxwell-main.sch

Title: MAXWELL Main Board

Size: A3	Date: 2020-07-16	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.4)		Id: 1/18


Sheet: Intermediate and Standby Rails
I2C2_SDA
I2C2_SCL
12V0
5V0_SB
3V3_SB
GND
File: intermediate-power.sch
Sheet: 1.xV rails
1V0_1
1V0_2
1V0_1_GOOD
1V0_2_GOOD
1V0_EN
1V2
1V2_GOOD
1V2_EN
1V5
1V5_GOOD
1V5_EN
1V8
1V8_GOOD
1V8_EN
RAM_VREF
RAM_VTT
VTT_GOOD
VTT_EN
0V5
0V5_EN
0V5_GOOD
File: 1v-rails.sch
Sheet: Higher voltage rails
5V0
5V0_GOOD
5V0_EN
5V0_N
5V0_N_EN
3V3
3V3_GOOD
3V3_EN
2V5
2V5_GOOD
2V5_EN
2V0
2V0_GOOD
2V0_EN
VBACKLIGHT_P
VBACKLIGHT_EN
VBACKLIGHT_N
BACKLIGHT_PWM
File: higher-rails.sch
U80
AT30TS74_UDFN
VCC
GND
A0
A1
A2
SDA
SCL
ALERT
Addr = 8'h98
TEMP1_ALERT
U81
Addr = 8'h9a
TEMP2_ALERT
U82
Addr = 8'h9c
TEMP3_ALERT
U83
Addr = 8'h9e
TEMP4_ALERT
C404
C405
C406
C407
0.47 uF
Rail design targets including safety margin
INPUT: 24-48V at 5A
Intermediate rail: 12V @ 9A
1V0: 8A
1V2: 1.5A
1V5: 6A
1V8: 1A
2V0: 500 mA
2V5: 1A
3V3: 3A
5V0: 100 mA
5V0N: 100 mA
12V0: 4A plus regulator inputs
21V5 for LCD: Constant current, nominally 33 mA
DDR RAM Vref, Vtt: standard regulator
Pullups for PGOOD signals in
case MCU pullups are too weak
R227
R228
R229
R230
R231
R232
R233
R235
R236
R237
DNP
1V0_1_GOOD
1V0_2_GOOD
1V2_GOOD
1V5_GOOD
1V8_GOOD
VTT_GOOD
0V5_GOOD
3V3_GOOD
2V5_GOOD
2V0_GOOD
Andrew D. Zonenberg
Antikernel Labs
Sheet: /Power Supply/
File: psu.sch
Title: MAXWELL Main Board
Size: A4
Date: 2020-07-16
Rev: 0.1
KiCad E.D.A. kicad (5.1.4)
Id: 2/18



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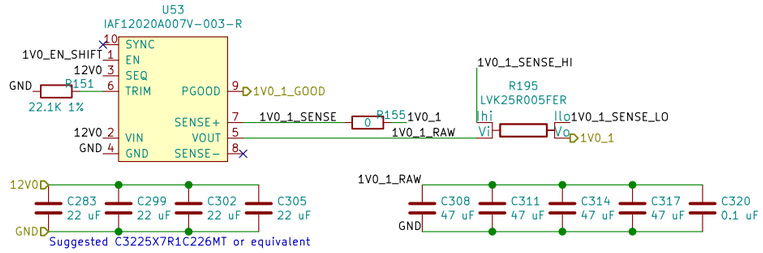
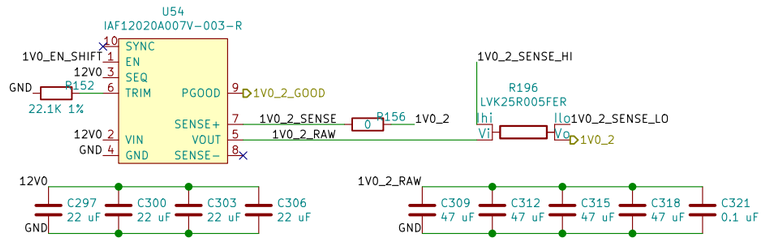
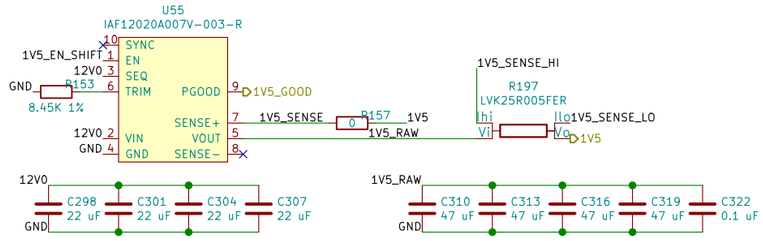
Sheet: /Power Supply/Intermediate and Standby Rails/
File: intermediate-power.sch

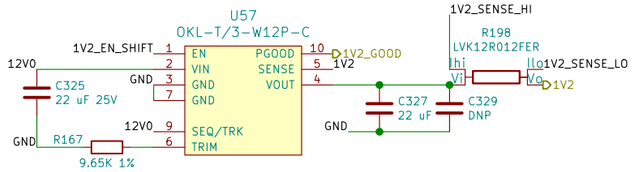
Title: MAXWELL Main Board

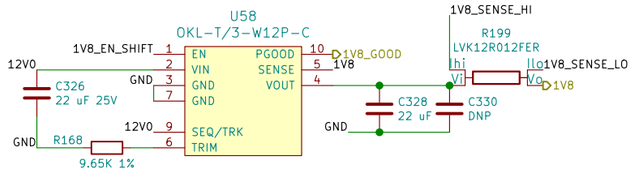
Size: A4	Date: 2020-07-16	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.4)		Id: 3/18



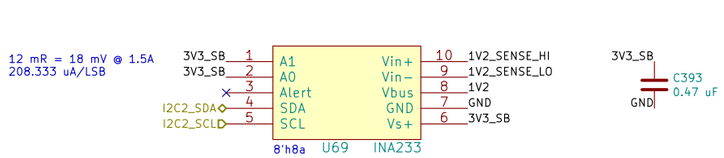


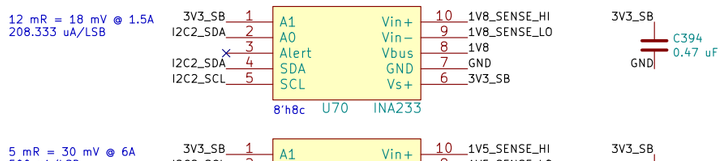


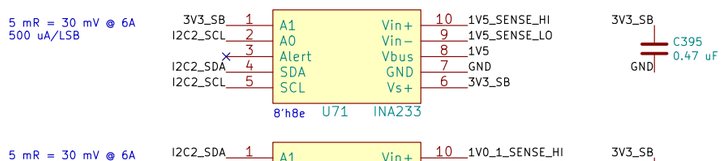


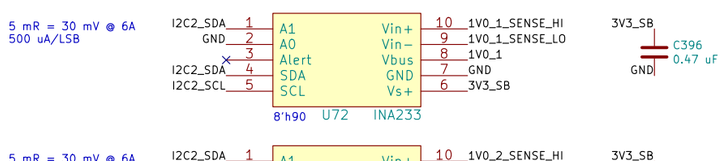


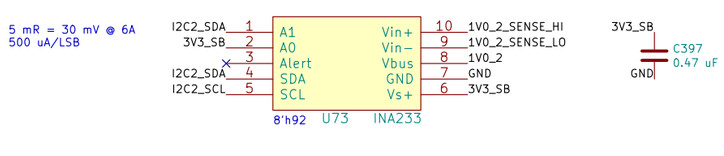
1.xV rails are max 6A
LVK25 are rated for 2W
6A through 5 mR = 180 mW max

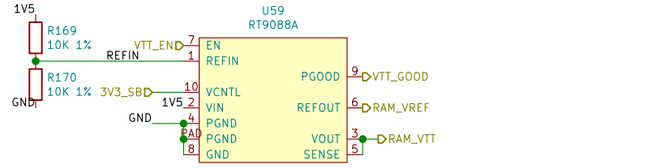


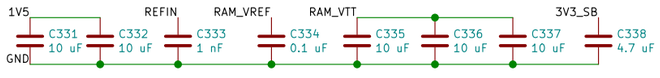


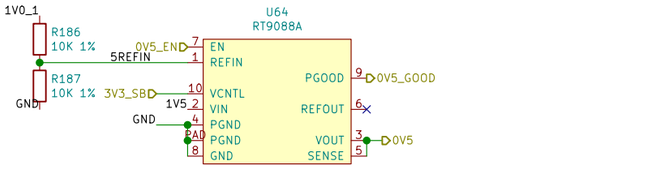


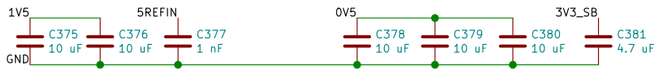




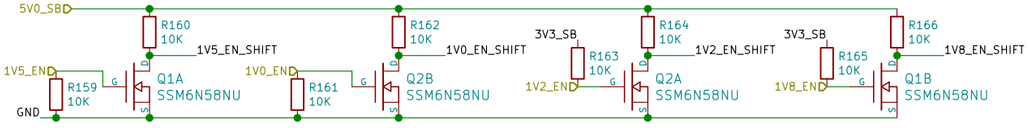








Regulator enables need >3.3V to switch on fully:
* IAFs need 4.2V min
* OKL-T/3 needs 3.5V min
Level shifter inverts, drive low to enable 1V2 or 1V8
1V5/1V0 are negative enable so after inversion, drive high to enable



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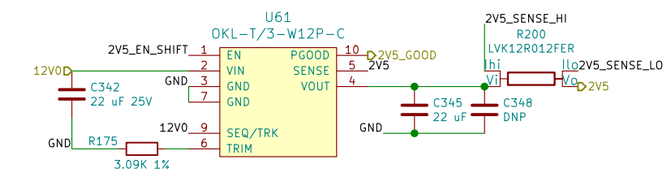
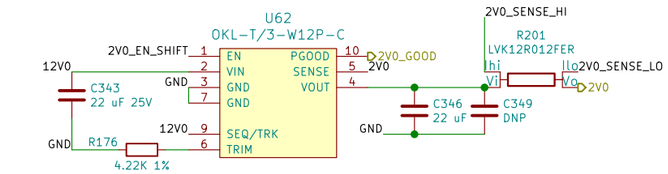
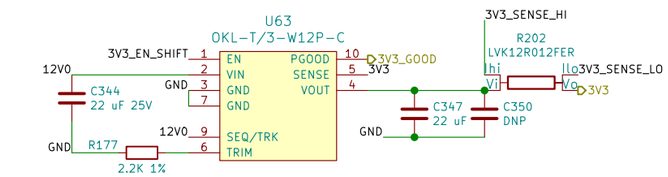
Sheet: /Power Supply/1.xV rails/
File: 1v-rails.sch

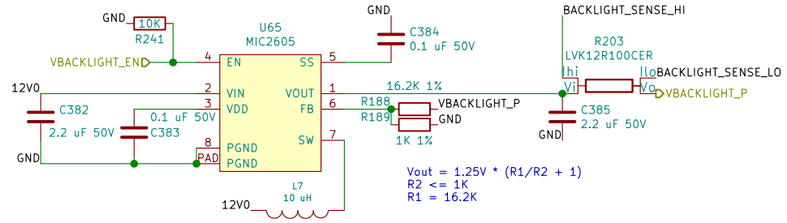
Title: MAXWELL Main Board

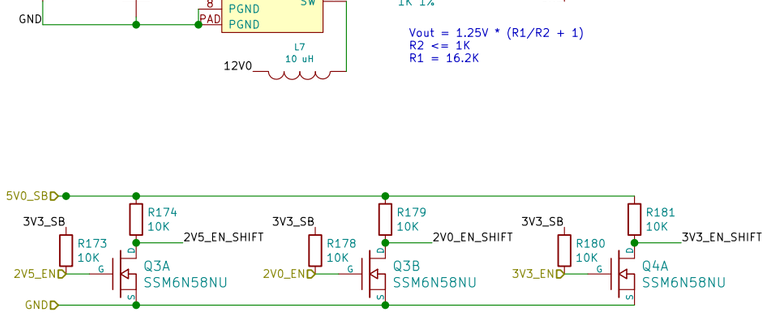
Size: A3	Date: 2020-07-16	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.4)		Id: 4/18









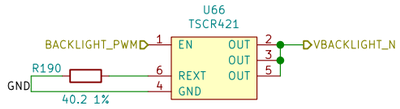


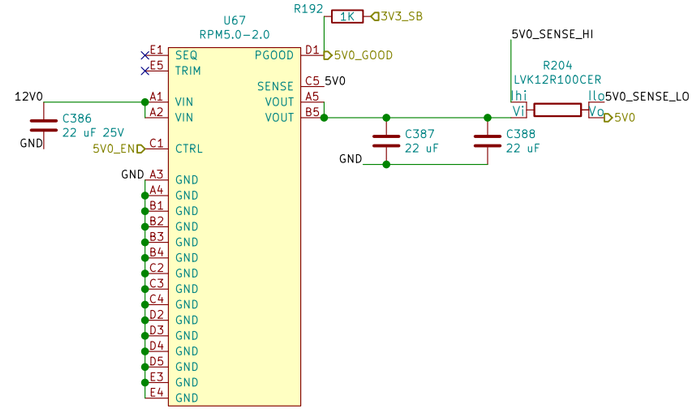
We want a total of ~40 mA
Backlight Vf is 17.4 – 19.8V @ 20 mA

Rext = Vdrop / (Iout – (Vdrop / Rint))

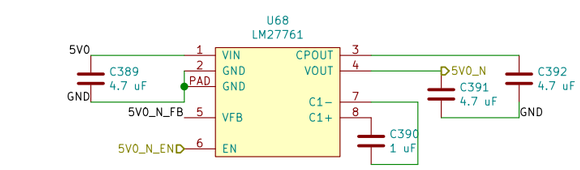
40 ohms gives 33.75 mA

Max 1W inst power, 150C, 225 C/W
Worst case Vf = 17.4V, dropping 4.1V = 138 mW, 31.05C rise
Best case 19.8V, dropping 1.7V = 58 mW, 13C rise

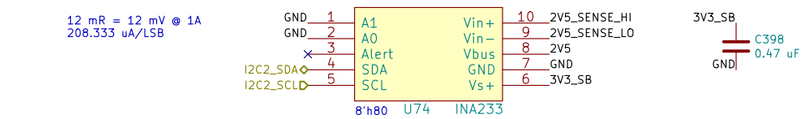


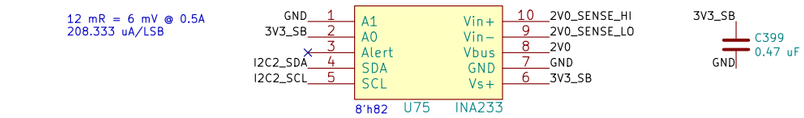


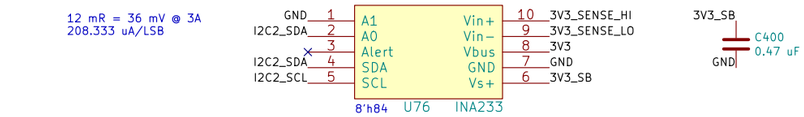
All rails here are max 3A
LVK12 is rated for 500 mW
3A through 12 mR is 108 mW

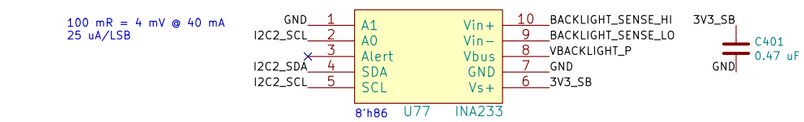


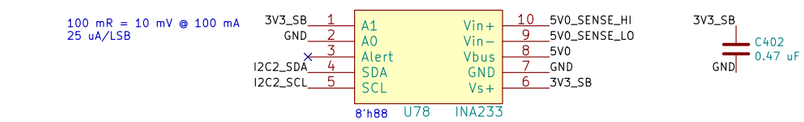
16 bits signed, 81.92 mV full scale
2.5 uV/LSB











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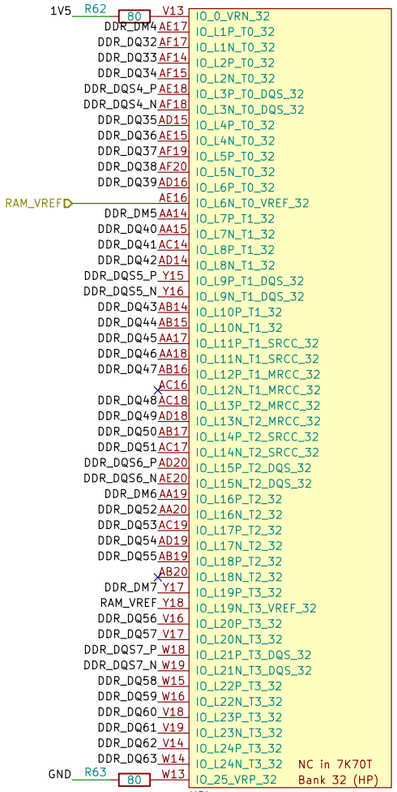
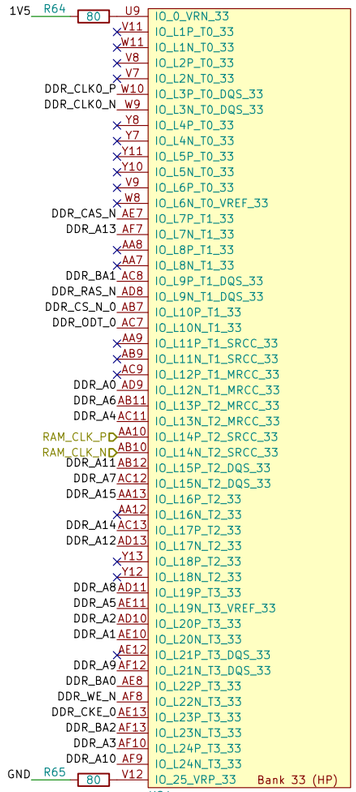
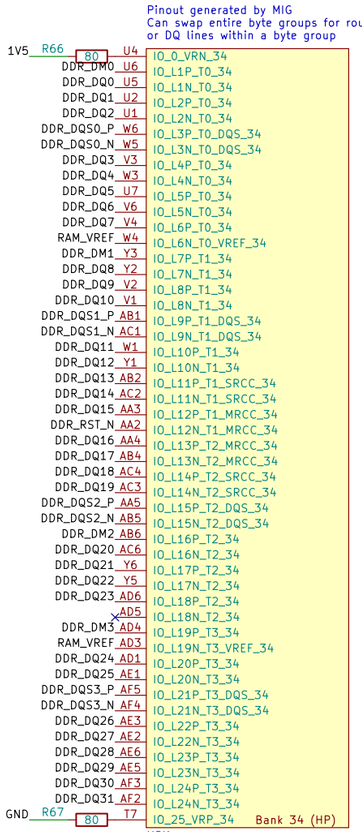
Sheet: /Power Supply/Higher voltage rails/
File: higher–rails.sch

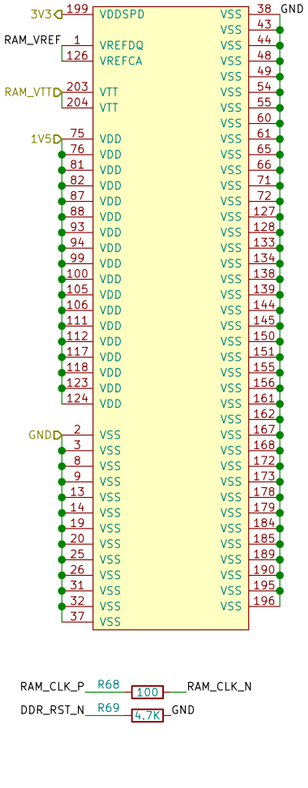
Title: MAXWELL Main Board

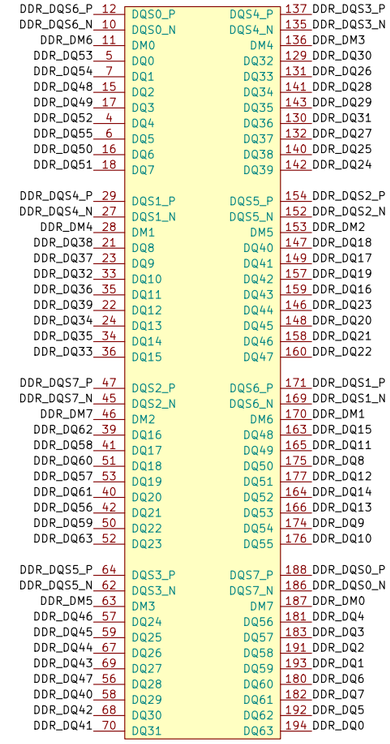
Size: A3	Date: 2020–07–16	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.4)		Id: 5/18

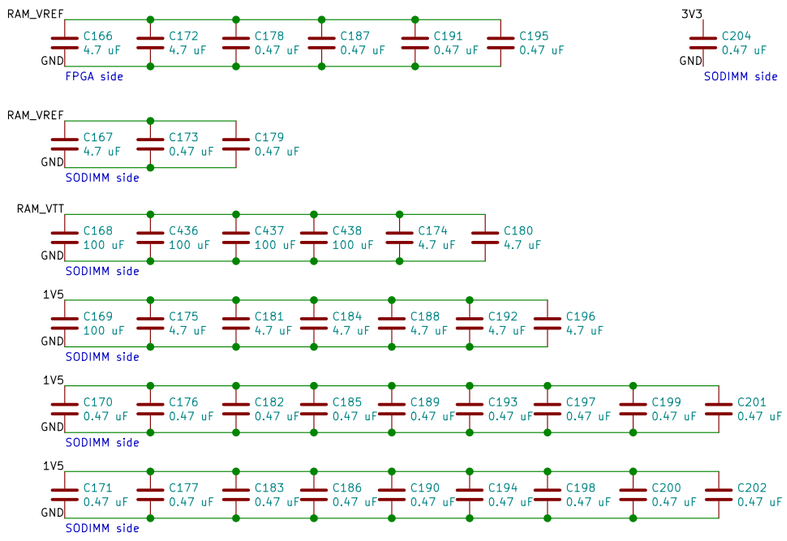


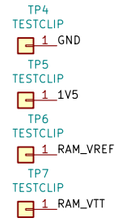












Route DQS and CK traces with 80 ohm impedance
Route DQ lines with 40 ohm impedance

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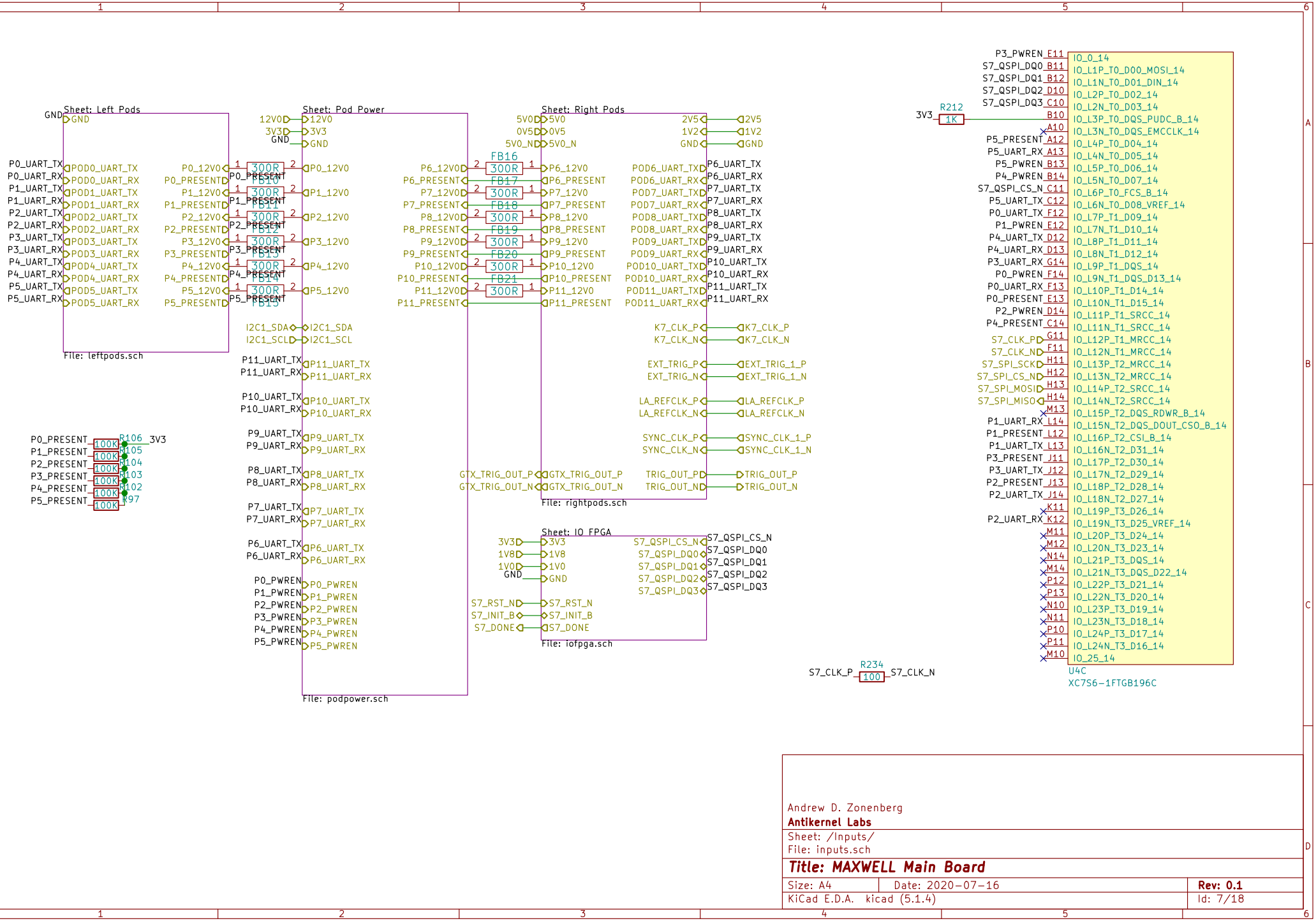
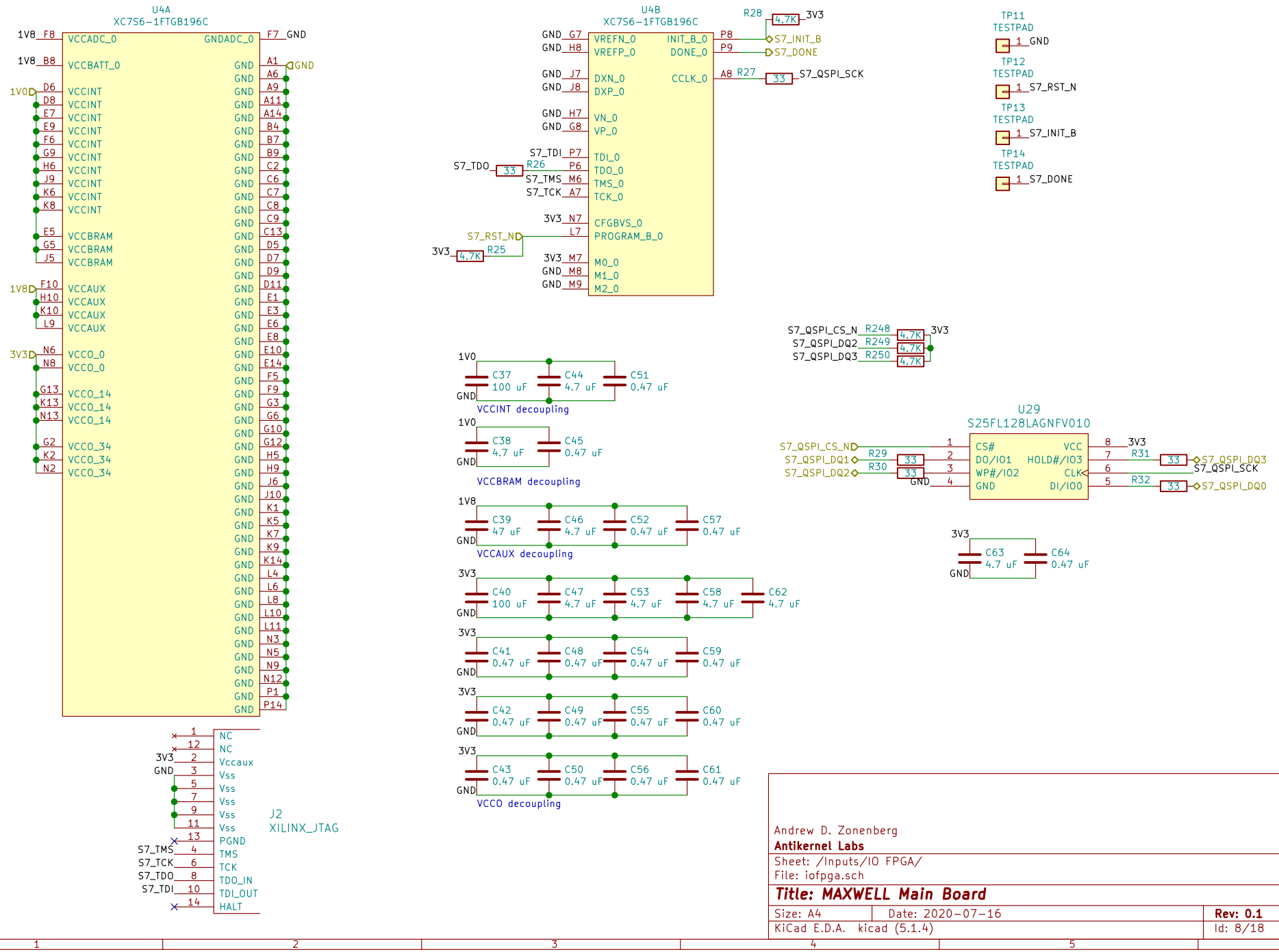
Sheet: /RAM/
File: ram.sch

Title: MAXWELL Main Board

Size: A3	Date: 2020-07-16	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.4)		Id: 6/18


Sheet: Left Pods
File: leftpods.sch
Sheet: Pod Power
File: podpower.sch
Sheet: Right Pods
File: rightpods.sch
Sheet: IO FPGA
File: iofpga.sch
U4C
XC7S6-1FTGB196C
Andrew D. Zonenberg
Antikernel Labs
Sheet: /Inputs/
File: inputs.sch
Title: MAXWELL Main Board
Size: A4
Date: 2020-07-16
Rev: 0.1
KiCad E.D.A. kicad (5.1.4)
Id: 7/18


U4A
XC7S6-1FTGB196C
U4B
XC7S6-1FTGB196C
TP11
TESTPAD
TP12
TESTPAD
TP13
TESTPAD
TP14
TESTPAD
U29
S25FL128LAGNFV010
J2
XILINX_JTAG
VCCINT decoupling
VCCBRAM decoupling
VCCAUX decoupling
VCCO decoupling
Andrew D. Zonenberg
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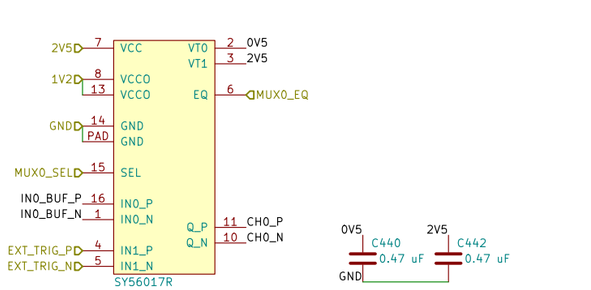
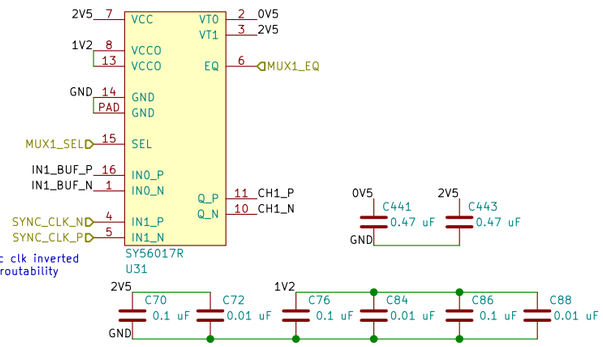
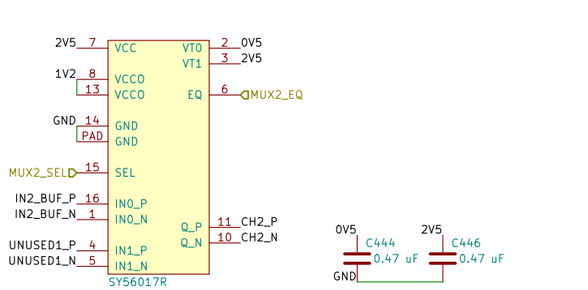
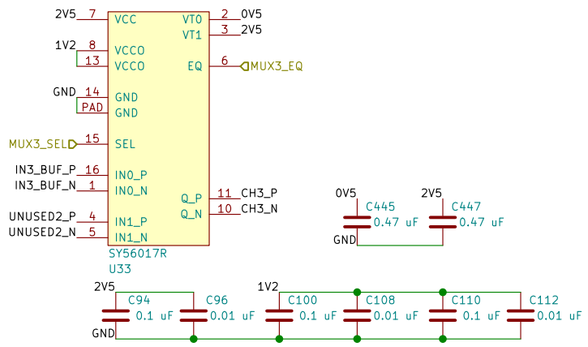
Sheet: /Inputs/IO FPGA/
File: iofpga.sch
Title: MAXWELL Main Board
Size: A4
Date: 2020-07-16
Rev: 0.1
KiCad E.D.A. kicad (5.1.4)
Id: 8/18

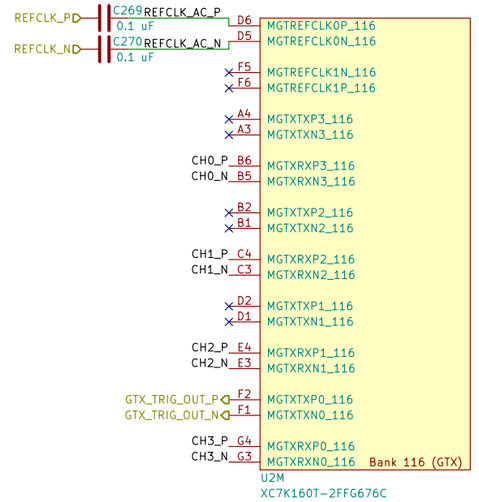

POD6_D0_P B2
POD6_D0_N B3
POD6_D1_P B5
POD6_D1_N B6
POD6_D2_P B13
POD6_D2_N B14
POD6_D3_P B16
POD6_D3_N B17
POD6_D4_P A2
POD6_D4_N A3
POD6_D5_P A5
POD6_D5_N A6
POD6_D6_P A13
POD6_D6_N A14
POD6_D7_P A16
POD6_D7_N A17
TX0_P
TX0_N
TX1_P
TX1_N
TX2_P
TX2_N
TX3_P
TX3_N
RX0_P
RX0_N
RX1_P
RX1_N
RX2_P
RX2_N
RX3_P
RX3_N
J3B
CONN_SFF8087
POD7_D0_P B2
POD7_D0_N B3
POD7_D1_P B5
POD7_D1_N B6
POD7_D2_P B13
POD7_D2_N B14
POD7_D3_P B16
POD7_D3_N B17
POD7_D4_P A2
POD7_D4_N A3
POD7_D5_P A5
POD7_D5_N A6
POD7_D6_P A13
POD7_D6_N A14
POD7_D7_P A16
POD7_D7_N A17
J4B
CONN_SFF8087
POD8_D0_P B2
POD8_D0_N B3
POD8_D1_P B5
POD8_D1_N B6
POD8_D2_P B13
POD8_D2_N B14
POD8_D3_P B16
POD8_D3_N B17
POD8_D4_P A2
POD8_D4_N A3
POD8_D5_P A5
POD8_D5_N A6
POD8_D6_P A13
POD8_D6_N A14
POD8_D7_P A16
POD8_D7_N A17
J5B
CONN_SFF8087
POD9_D0_P B2
POD9_D0_N B3
POD9_D1_P B5
POD9_D1_N B6
POD9_D2_P B13
POD9_D2_N B14
POD9_D3_P B16
POD9_D3_N B17
POD9_D4_P A2
POD9_D4_N A3
POD9_D5_P A5
POD9_D5_N A6
POD9_D6_P A13
POD9_D6_N A14
POD9_D7_P A16
POD9_D7_N A17
J6B
CONN_SFF8087
POD10_D0_P B2
POD10_D0_N B3
POD10_D1_P B5
POD10_D1_N B6
POD10_D2_P B13
POD10_D2_N B14
POD10_D3_P B16
POD10_D3_N B17
POD10_D4_P A2
POD10_D4_N A3
POD10_D5_P A5
POD10_D5_N A6
POD10_D6_P A13
POD10_D6_N A14
POD10_D7_P A16
POD10_D7_N A17
J7B
CONN_SFF8087
POD11_D0_P B2
POD11_D0_N B3
POD11_D1_P B5
POD11_D1_N B6
POD11_D2_P B13
POD11_D2_N B14
POD11_D3_P B16
POD11_D3_N B17
POD11_D4_P A2
POD11_D4_N A3
POD11_D5_P A5
POD11_D5_N A6
POD11_D6_P A13
POD11_D6_N A14
POD11_D7_P A16
POD11_D7_N A17
J8B
CONN_SFF8087
P6_12V0 B8
B9
B10
POD6_UART_TX A9
P6_PRESENT A10
P6_12V0 A11
POD6_UART_RX A8
P6_12V0 B11
SB0
SB1
SB2
SB3
SB4
SB5
SB6
SB7
GND B1
A1
B4
A4
B7
A7
B12
C12
C15
A15
A18
GND
SHLD
J3A
CONN_SFF8087
P7_12V0 B8
B9
B10
POD7_UART_TX A9
P7_PRESENT A10
P7_12V0 A11
POD7_UART_RX A8
P7_12V0 B11
J4A
CONN_SFF8087
P8_12V0 B8
B9
B10
POD8_UART_TX A9
P8_PRESENT A10
P8_12V0 A11
POD8_UART_RX A8
P8_12V0 B11
J5A
CONN_SFF8087
P9_12V0 B8
B9
B10
POD9_UART_TX A9
P9_PRESENT A10
P9_12V0 A11
POD9_UART_RX A8
P9_12V0 B11
J6A
CONN_SFF8087
P10_12V0 B8
B9
B10
POD10_UART_TX A9
P10_PRESENT A10
P10_12V0 A11
POD10_UART_RX A8
P10_12V0 B11
J7A
CONN_SFF8087
P11_12V0 B8
B9
B10
POD11_UART_TX A9
P11_PRESENT A10
P11_12V0 A11
POD11_UART_RX A8
P11_12V0 B11
J8A
CONN_SFF8087
D2
ESD7008
POD6_D0_P 1
POD6_D0_N 2
POD6_D1_P 4
POD6_D1_N 5
POD6_D2_P 7
POD6_D2_N 8
POD6_D3_P 10
POD6_D3_N 11
IO
GND 3 6 9 13 15 17
GND
D3
ESD7008
POD6_D7_N 1
POD6_D7_P 2
POD6_D6_N 4
POD6_D6_P 5
POD6_D5_N 7
POD6_D5_P 8
POD6_D4_N 10
POD6_D4_P 11
D4
ESD7008
POD7_D0_P 1
POD7_D0_N 2
POD7_D1_P 4
POD7_D1_N 5
POD7_D2_P 7
POD7_D2_N 8
POD7_D3_P 10
POD7_D3_N 11
D5
ESD7008
POD7_D7_N 1
POD7_D7_P 2
POD7_D6_N 4
POD7_D6_P 5
POD7_D5_N 7
POD7_D5_P 8
POD7_D4_N 10
POD7_D4_P 11
D6
ESD7008
POD8_D0_P 1
POD8_D0_N 2
POD8_D1_P 4
POD8_D1_N 5
POD8_D2_P 7
POD8_D2_N 8
POD8_D3_P 10
POD8_D3_N 11
D7
ESD7008
POD8_D7_N 1
POD8_D7_P 2
POD8_D6_N 4
POD8_D6_P 5
POD8_D5_N 7
POD8_D5_P 8
POD8_D4_N 10
POD8_D4_P 11
D8
ESD7008
POD9_D0_P 1
POD9_D0_N 2
POD9_D1_P 4
POD9_D1_N 5
POD9_D2_P 7
POD9_D2_N 8
POD9_D3_P 10
POD9_D3_N 11
D9
ESD7008
POD9_D7_N 1
POD9_D7_P 2
POD9_D6_N 4
POD9_D6_P 5
POD9_D5_N 7
POD9_D5_P 8
POD9_D4_N 10
POD9_D4_P 11
D10
ESD7008
POD10_D0_P 1
POD10_D0_N 2
POD10_D1_P 4
POD10_D1_N 5
POD10_D2_P 7
POD10_D2_N 8
POD10_D3_P 10
POD10_D3_N 11
D11
ESD7008
POD10_D7_N 1
POD10_D7_P 2
POD10_D6_N 4
POD10_D6_P 5
POD10_D5_N 7
POD10_D5_P 8
POD10_D4_N 10
POD10_D4_P 11
D12
ESD7008
POD11_D0_P 1
POD11_D0_N 2
POD11_D1_P 4
POD11_D1_N 5
POD11_D2_P 7
POD11_D2_N 8
POD11_D3_P 10
POD11_D3_N 11
D13
ESD7008
POD11_D7_N 1
POD11_D7_P 2
POD11_D6_N 4
POD11_D6_P 5
POD11_D5_N 7
POD11_D5_P 8
POD11_D4_N 10
POD11_D4_P 11
D30
ESD7008
POD6_UART_RX 1
POD6_UART_TX 2
P6_PRESENT 4
5
7
POD7_UART_RX 8
POD7_UART_TX 10
P7_PRESENT 11
D31
ESD7008
POD8_UART_RX 1
POD8_UART_TX 2
P8_PRESENT 4
5
7
POD9_UART_RX 8
POD9_UART_TX 10
P9_PRESENT 11
D32
ESD7008
POD10_UART_RX 1
POD10_UART_TX 2
P10_PRESENT 4
5
7
POD11_UART_RX 8
POD11_UART_TX 10
P11_PRESENT 11
Polarity swap for routability:
* POD11_D3
* POD11_D1
* POD11_D0
* POD10_D7
* POD10_D6
* POD10_D5
* POD10_D2
* POD10_D1
* POD10_D0
* POD9_D4
* POD8_D4
* POD7_D7
* POD7_D6
* POD7_D5
* POD7_D1
* POD6_D7
* POD6_D5
* POD6_D3
* POD6_D2
Sheet: SERDES inputs
POD11_D4_P
POD11_D4_N
POD11_D5_P
POD11_D5_N
POD11_D6_P
POD11_D6_N
POD11_D7_P
POD11_D7_N
IN0_P
IN0_N
IN1_P
IN1_N
IN2_P
IN2_N
IN3_P
IN3_N
EXT_TRIG_P
EXT_TRIG_N
LA_REFCLK_P
LA_REFCLK_N
SYNC_CLK_P
SYNC_CLK_N
GTX_TRIG_OUT_P
GTX_TRIG_OUT_N
REFCLK_P
REFCLK_N
5V0
2V5
1V2
0V5
GND
5V0_N
MUX0_SEL
MUX0_EQ
MUX1_SEL
MUX1_EQ
MUX2_SEL
MUX2_EQ
MUX3_SEL
MUX3_EQ
File: serdesinputs.sch
MUX2_EQ K15
POD7_D3_P C16
POD7_D3_N B16
POD7_D1_N A18
POD7_D1_P A19
POD7_D2_P B17
POD7_D2_N A17
POD7_D0_P C19
POD7_D0_N B19
POD7_D5_N C17
POD7_D5_P C18
POD7_D7_N D15
POD7_D7_P D16
POD10_D6_N H16
POD10_D6_P G16
POD10_D7_N G15
POD10_D7_P F15
POD10_D2_N J15
POD10_D2_P J16
POD8_D4_N E15
POD8_D4_P E16
POD10_D0_N G17
POD10_D0_P F18
POD7_D6_N F17
POD7_D6_P E17
POD7_D4_P E18
POD7_D4_N D18
POD10_D5_N H17
POD10_D5_P H18
MUX3_EQ D19
MUX3_SEL D20
POD6_D1_P G19
POD6_D1_N F20
POD6_D2_N F19
POD6_D2_P E20
POD6_D0_P H19
POD6_D0_N G20
POD6_D6_P K20
POD6_D6_N J20
POD6_D7_N J18
POD6_D7_P J19
POD6_D5_N L19
POD6_D5_P L20
POD10_D1_N K16
POD10_D1_P K17
POD6_D4_P M17
POD6_D4_N L18
POD6_D3_N L17
POD6_D3_P K18
MUX2_SEL M16
IO_0_15
IO_L1P_T0_AD0P_15
IO_L1N_T0_AD0N_15
IO_L2P_T0_AD8P_15
IO_L2N_T0_AD8N_15
IO_L3P_T0_DQS_AD1P_15
IO_L3N_T0_DQS_AD1N_15
IO_L4P_T0_AD9P_15
IO_L4N_T0_AD9N_15
IO_L5P_T0_AD2P_15
IO_L5N_T0_AD2N_15
IO_L6P_T0_15
IO_L6N_T0_VREF_15
IO_L7P_T1_AD10P_15
IO_L7N_T1_AD10N_15
IO_L8P_T1_AD3P_15
IO_L8N_T1_AD3N_15
IO_L9P_T1_DQS_AD11P_15
IO_L9N_T1_DQS_AD11N_15
IO_L10P_T1_AD4P_15
IO_L10N_T1_AD4N_15
IO_L11P_T1_SRCC_AD12P_15
IO_L11N_T1_SRCC_AD12N_15
IO_L12P_T1_MRCC_AD5P_15
IO_L12N_T1_MRCC_AD5N_15
IO_L13P_T2_MRCC_15
IO_L13N_T2_MRCC_15
IO_L14P_T2_SRCC_15
IO_L14N_T2_SRCC_15
IO_L15P_T2_DQS_15
IO_L15N_T2_DQS_ADV_B_15
IO_L16P_T2_A28_15
IO_L16N_T2_A27_15
IO_L17P_T2_A26_15
IO_L17N_T2_A25_15
IO_L18P_T2_A24_15
IO_L18N_T2_A23_15
IO_L19P_T3_A22_15
IO_L19N_T3_A21_VREF_15
IO_L20P_T3_A20_15
IO_L20N_T3_A19_15
IO_L21P_T3_DQS_15
IO_L21N_T3_DQS_A18_15
IO_L22P_T3_A17_15
IO_L22N_T3_A16_15
IO_L23P_T3_FOE_B_15
IO_L23N_T3_FWE_B_15
IO_L24P_T3_RS1_15
IO_L24N_T3_RS0_15
IO_25_15
Bank 15 (HR)
U2G
XC7K160T-2FFG676C
MUX1_EQ J8
TRIG_OUT_P H9
TRIG_OUT_N H8
POD9_D5_P G10
POD9_D5_N G9
POD11_D3_N J13
POD11_D3_P H13
POD11_D2_P J11
POD11_D2_N J10
POD11_D1_N H14
POD11_D1_P G14
POD10_D4_P H12
POD10_D4_N H11
POD9_D7_P F9
POD9_D7_N F8
POD9_D6_P D9
POD9_D6_N D8
POD9_D3_P A9
POD9_D3_N A8
POD9_D2_P C9
POD9_D2_N B9
POD11_D0_N G11
POD11_D0_P F10
K7_CLK_PD E10
K7_CLK_ND D10
POD8_D7_P C12
POD8_D7_N C11
POD9_D4_N E11
POD9_D4_P D11
POD10_D3_P F14
POD10_D3_N F13
MUX0_SEL G12
MUX1_SEL F12
POD8_D5_P D14
POD8_D5_N D13
POD8_D6_P E13
POD8_D6_N E12
POD8_D2_P C14
POD8_D2_N C13
POD9_D0_P B12
POD9_D0_N B11
POD8_D1_P B14
POD8_D1_N A14
POD9_D1_P B10
POD9_D1_N A10
POD8_D0_P B15
POD8_D0_N A15
POD8_D3_P A13
POD8_D3_N A12
MUX0_EQ J14
IO_0_16
IO_L1P_T0_16
IO_L1N_T0_16
IO_L2P_T0_16
IO_L2N_T0_16
IO_L3P_T0_DQS_16
IO_L3N_T0_DQS_16
IO_L4P_T0_16
IO_L4N_T0_16
IO_L5P_T0_16
IO_L5N_T0_16
IO_L6P_T0_16
IO_L6N_T0_VREF_16
IO_L7P_T1_16
IO_L7N_T1_16
IO_L8P_T1_16
IO_L8N_T1_16
IO_L9P_T1_DQS_16
IO_L9N_T1_DQS_16
IO_L10P_T1_16
IO_L10N_T1_16
IO_L11P_T1_SRCC_16
IO_L11N_T1_SRCC_16
IO_L12P_T1_MRCC_16
IO_L12N_T1_MRCC_16
IO_L13P_T2_MRCC_16
IO_L13N_T2_MRCC_16
IO_L14P_T2_SRCC_16
IO_L14N_T2_SRCC_16
IO_L15P_T2_DQS_16
IO_L15N_T2_DQS_16
IO_L16P_T2_16
IO_L16N_T2_16
IO_L17P_T2_16
IO_L17N_T2_16
IO_L18P_T2_16
IO_L18N_T2_16
IO_L19P_T3_16
IO_L19N_T3_VREF_16
IO_L20P_T3_16
IO_L20N_T3_16
IO_L21P_T3_DQS_16
IO_L21N_T3_DQS_16
IO_L22P_T3_16
IO_L22N_T3_16
IO_L23P_T3_16
IO_L23N_T3_16
IO_L24P_T3_16
IO_L24N_T3_16
IO_25_16
Bank 16 (HR)
U2H
XC7K160T-2FFG676C
Andrew D. Zonenberg
Antikernel Labs
Sheet: /Inputs/Right Pods/
File: rightpods.sch
Title: MAXWELL Main Board
Size: A3
Date: 2020-07-16
Rev: 0.1
KiCad E.D.A. kicad (5.1.4)
Id: 9/18

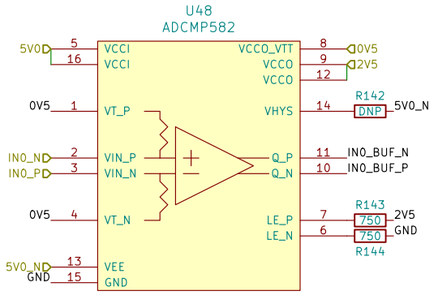


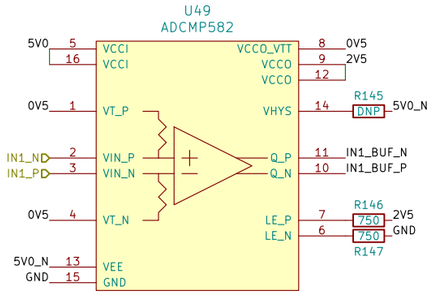


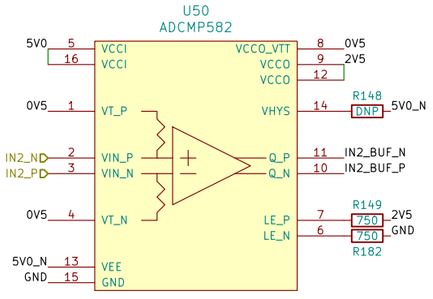


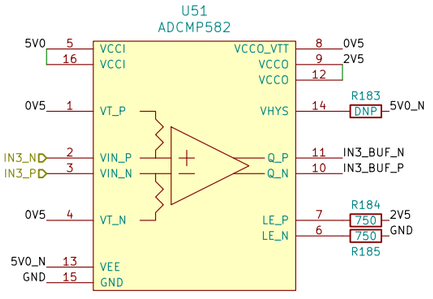












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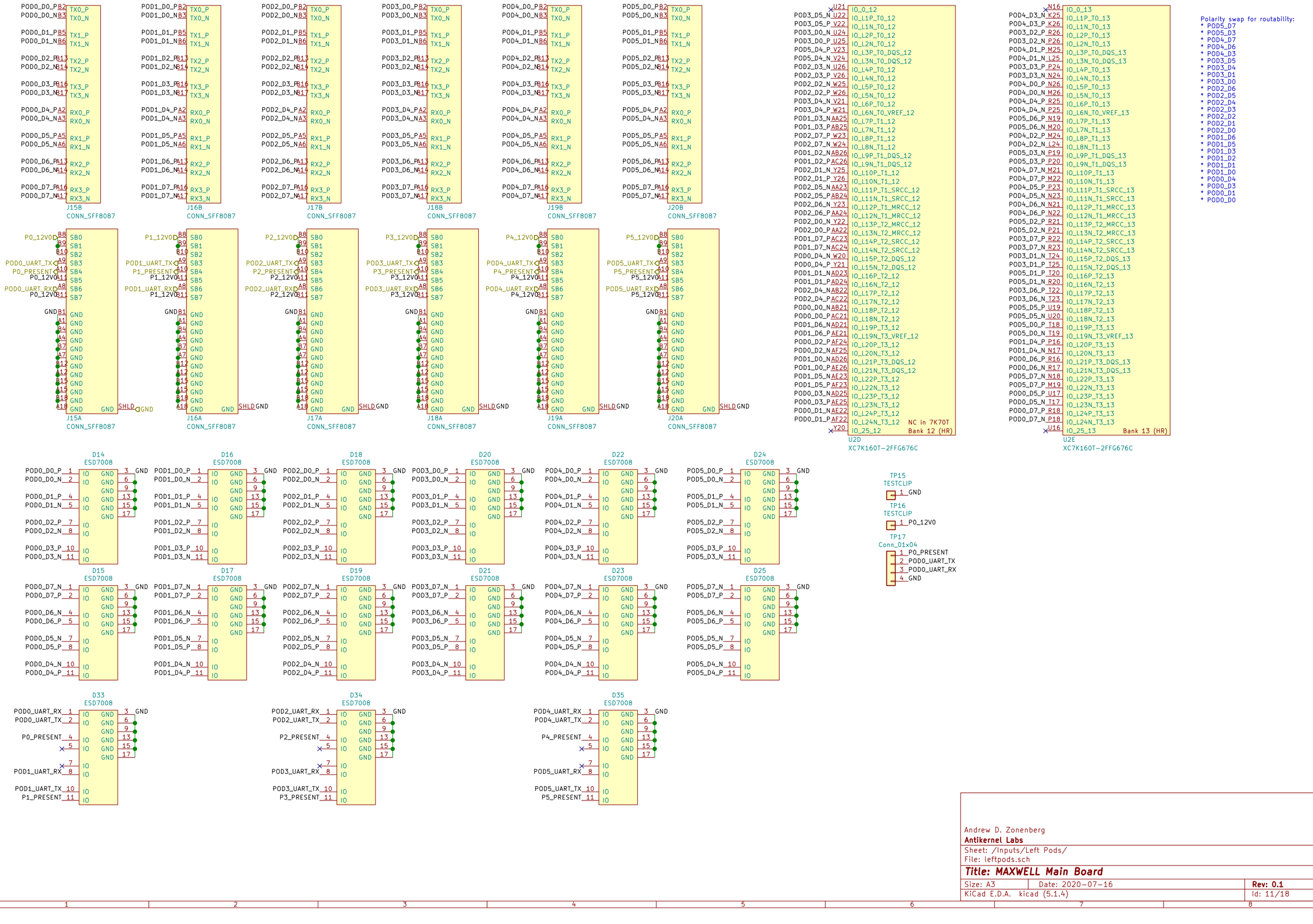
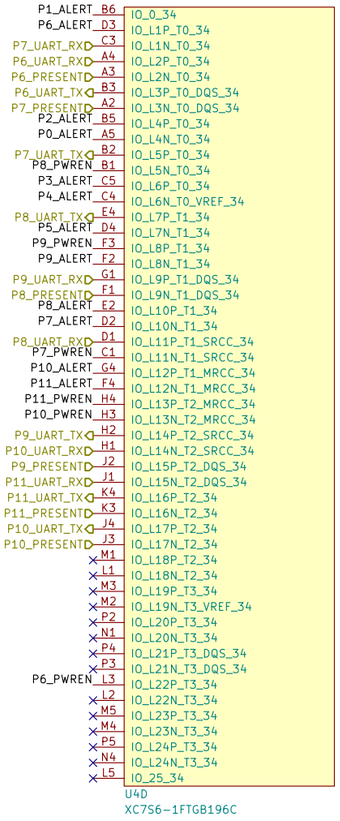
Sheet: /Inputs/Right Pods/SERDES inputs/
File: serdesinputs.sch

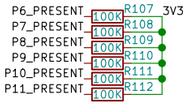
Title: MAXWELL Main Board

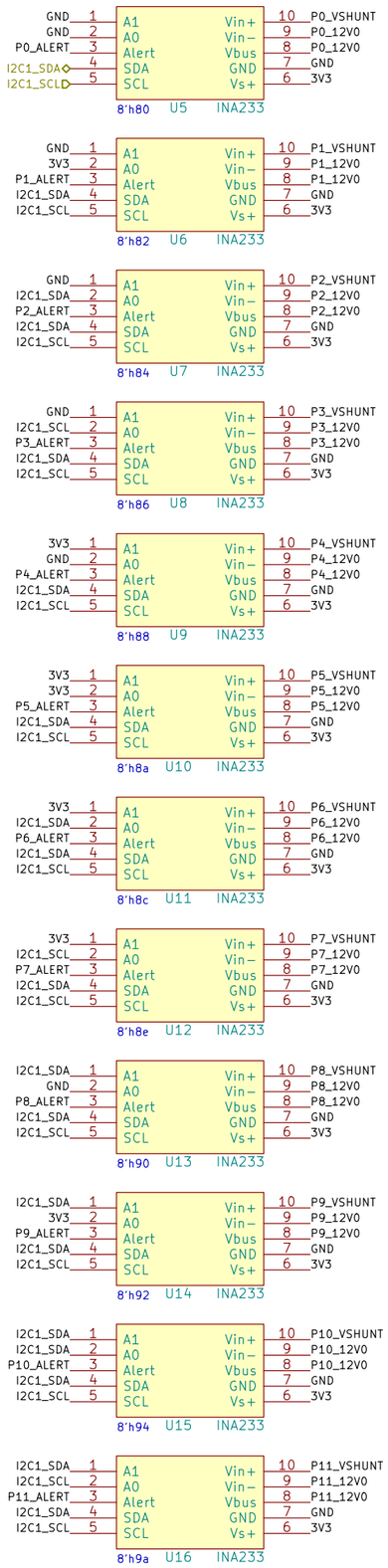
Size: A3	Date: 2020-07-16	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.4)		Id: 10/18


J15B CONN_SFF8087
J16B CONN_SFF8087
J17B CONN_SFF8087
J18B CONN_SFF8087
J19B CONN_SFF8087
J20B CONN_SFF8087
J15A CONN_SFF8087
J16A CONN_SFF8087
J17A CONN_SFF8087
J18A CONN_SFF8087
J19A CONN_SFF8087
J20A CONN_SFF8087
U2D XC7K160T-2FFG676C
NC in 7K70T
Bank 12 (HR)
U2E XC7K160T-2FFG676C
Bank 13 (HR)
Polarity swap for routability:
* POD5_D7
* POD5_D3
* POD4_D7
* POD4_D6
* POD4_D3
* POD3_D5
* POD3_D4
* POD3_D1
* POD3_D0
* POD2_D6
* POD2_D5
* POD2_D4
* POD2_D3
* POD2_D2
* POD2_D1
* POD2_D0
* POD1_D6
* POD1_D5
* POD1_D3
* POD1_D2
* POD1_D1
* POD1_D0
* POD0_D4
* POD0_D3
* POD0_D1
* POD0_D0
D14 ESD7008
D16 ESD7008
D18 ESD7008
D20 ESD7008
D22 ESD7008
D24 ESD7008
D15 ESD7008
D17 ESD7008
D19 ESD7008
D21 ESD7008
D23 ESD7008
D25 ESD7008
D33 ESD7008
D34 ESD7008
D35 ESD7008
TP15 TESTCLIP
TP16 TESTCLIP
TP17 Conn_01x04
P0_12V0
P0_PRESENT
PODO_UART_TX
PODO_UART_RX
GND
Andrew D. Zonenberg
Antikernel Labs
Sheet: /Inputs/Left Pods/
File: leftpods.sch
Title: MAXWELL Main Board
Size: A3
Date: 2020-07-16
Rev: 0.1
KiCad E.D.A. kicad (5.1.4)
Id: 11/18

Current Monitoring

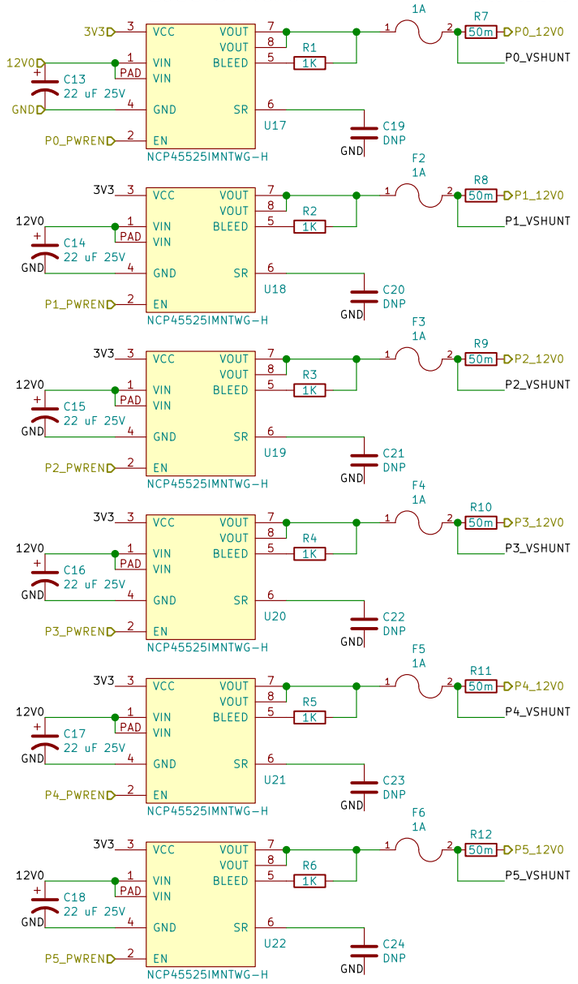


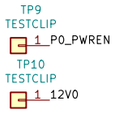




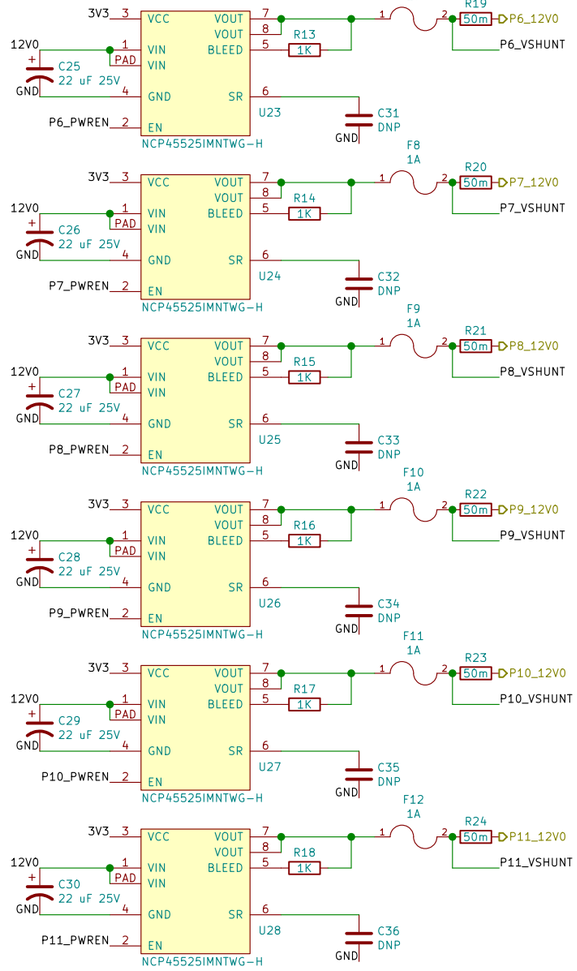
Load Switches

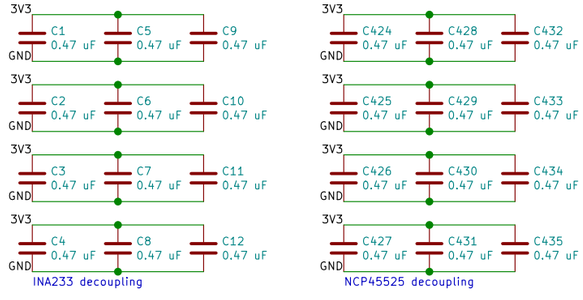
50m @ 1A = 50 mW
KDV06FR050ET is rated for 200





Bleed resistor is ~100 ohms.
Max safe power limit is 400 mW or 63 mA.
1K ohms gives ~10 mA, which is well below safe limits.
External resistor dissipates 100 mW, at the upper limit for an 0402, but only briefly during shutdown.





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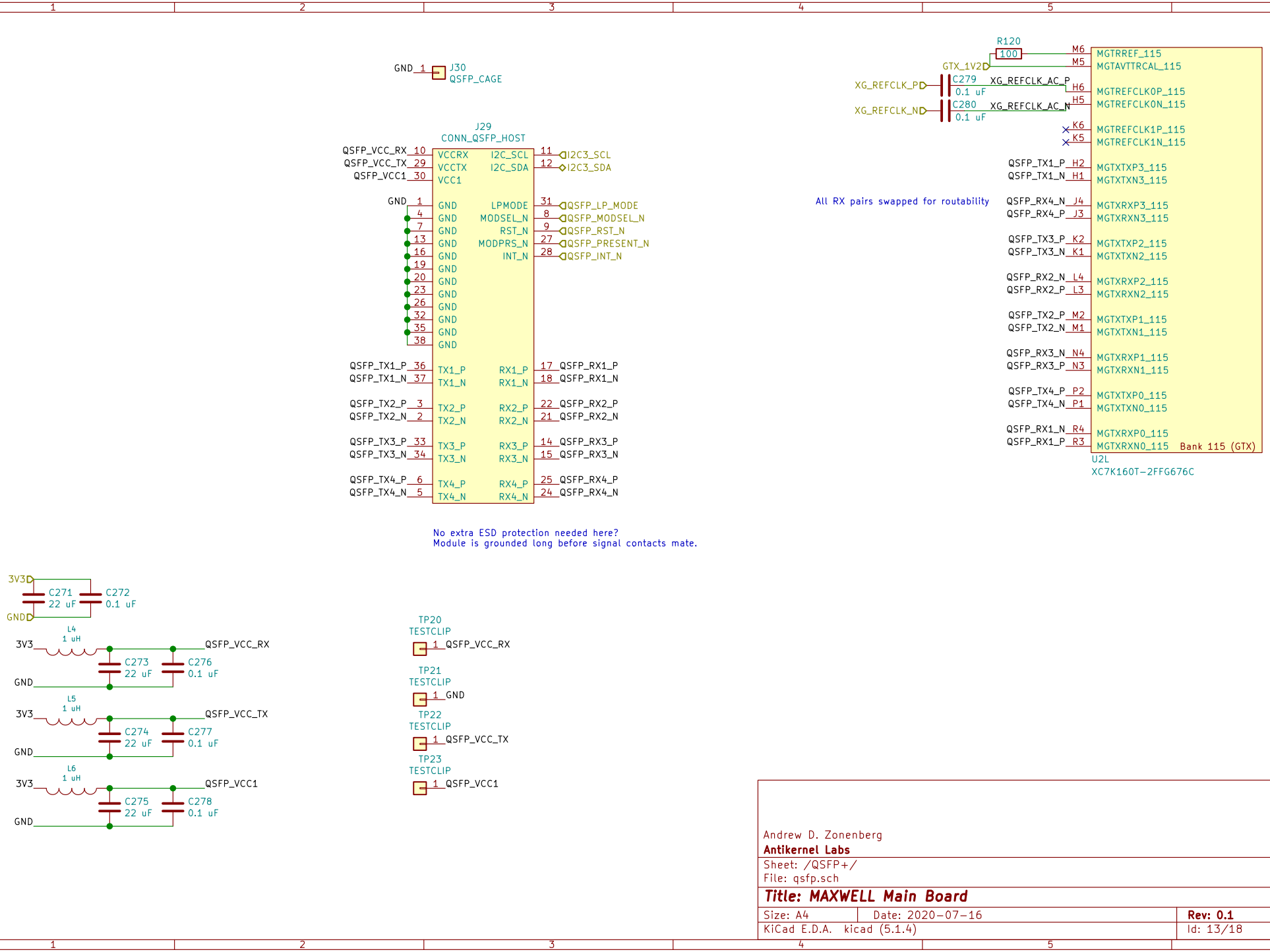
Sheet: /Inputs/Pod Power/
File: podpower.sch

Title: MAXWELL Main Board

Size: A3	Date: 2020-07-16	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.4)		Id: 12/18


GND 1 J30 QSFP_CAGE
J29 CONN_QSFP_HOST
QSFP_VCC_RX 10 VCCRX I2C_SCL 11 I2C3_SCL
QSFP_VCC_TX 29 VCCTX I2C_SDA 12 I2C3_SDA
QSFP_VCC1 30 VCC1
GND 1 GND LPMODE 31 QSFP_LP_MODE
4 GND MODSEL_N 8 QSFP_MODSEL_N
7 GND RST_N 9 QSFP_RST_N
13 GND MODPRS_N 27 QSFP_PRESENT_N
16 GND INT_N 28 QSFP_INT_N
19 GND
20 GND
23 GND
26 GND
32 GND
35 GND
38 GND
QSFP_TX1_P 36 TX1_P RX1_P 17 QSFP_RX1_P
QSFP_TX1_N 37 TX1_N RX1_N 18 QSFP_RX1_N
QSFP_TX2_P 3 TX2_P RX2_P 22 QSFP_RX2_P
QSFP_TX2_N 2 TX2_N RX2_N 21 QSFP_RX2_N
QSFP_TX3_P 33 TX3_P RX3_P 14 QSFP_RX3_P
QSFP_TX3_N 34 TX3_N RX3_N 15 QSFP_RX3_N
QSFP_TX4_P 6 TX4_P RX4_P 25 QSFP_RX4_P
QSFP_TX4_N 5 TX4_N RX4_N 24 QSFP_RX4_N
No extra ESD protection needed here?
Module is grounded long before signal contacts mate.
R120 100
GTX_1V2
XG_REFCLK_P C279 0.1 uF XG_REFCLK_AC_P
XG_REFCLK_N C280 0.1 uF XG_REFCLK_AC_N
All RX pairs swapped for routability
M6 MGTRREF_115
M5 MGTAVTTRCAL_115
H6 MGTREFCLK0P_115
H5 MGTREFCLK0N_115
K6 MGTREFCLK1P_115
K5 MGTREFCLK1N_115
QSFP_TX1_P H2 MGTXTXP3_115
QSFP_TX1_N H1 MGTXTXN3_115
QSFP_RX4_N J4 MGTXRXP3_115
QSFP_RX4_P J3 MGTXRXN3_115
QSFP_TX3_P K2 MGTXTXP2_115
QSFP_TX3_N K1 MGTXTXN2_115
QSFP_RX2_N L4 MGTXRXP2_115
QSFP_RX2_P L3 MGTXRXN2_115
QSFP_TX2_P M2 MGTXTXP1_115
QSFP_TX2_N M1 MGTXTXN1_115
QSFP_RX3_N N4 MGTXRXP1_115
QSFP_RX3_P N3 MGTXRXN1_115
QSFP_TX4_P P2 MGTXTXP0_115
QSFP_TX4_N P1 MGTXTXN0_115
QSFP_RX1_N R4 MGTXRXP0_115
QSFP_RX1_P R3 MGTXRXN0_115 Bank 115 (GTX)
U2L
XC7K160T-2FFG676C
3V3 C271 22 uF C272 0.1 uF GND
L4 1 uH 3V3 QSFP_VCC_RX C273 22 uF C276 0.1 uF GND
L5 1 uH 3V3 QSFP_VCC_TX C274 22 uF C277 0.1 uF GND
L6 1 uH 3V3 QSFP_VCC1 C275 22 uF C278 0.1 uF GND
TP20 TESTCLIP 1 QSFP_VCC_RX
TP21 TESTCLIP 1 GND
TP22 TESTCLIP 1 QSFP_VCC_TX
TP23 TESTCLIP 1 QSFP_VCC1
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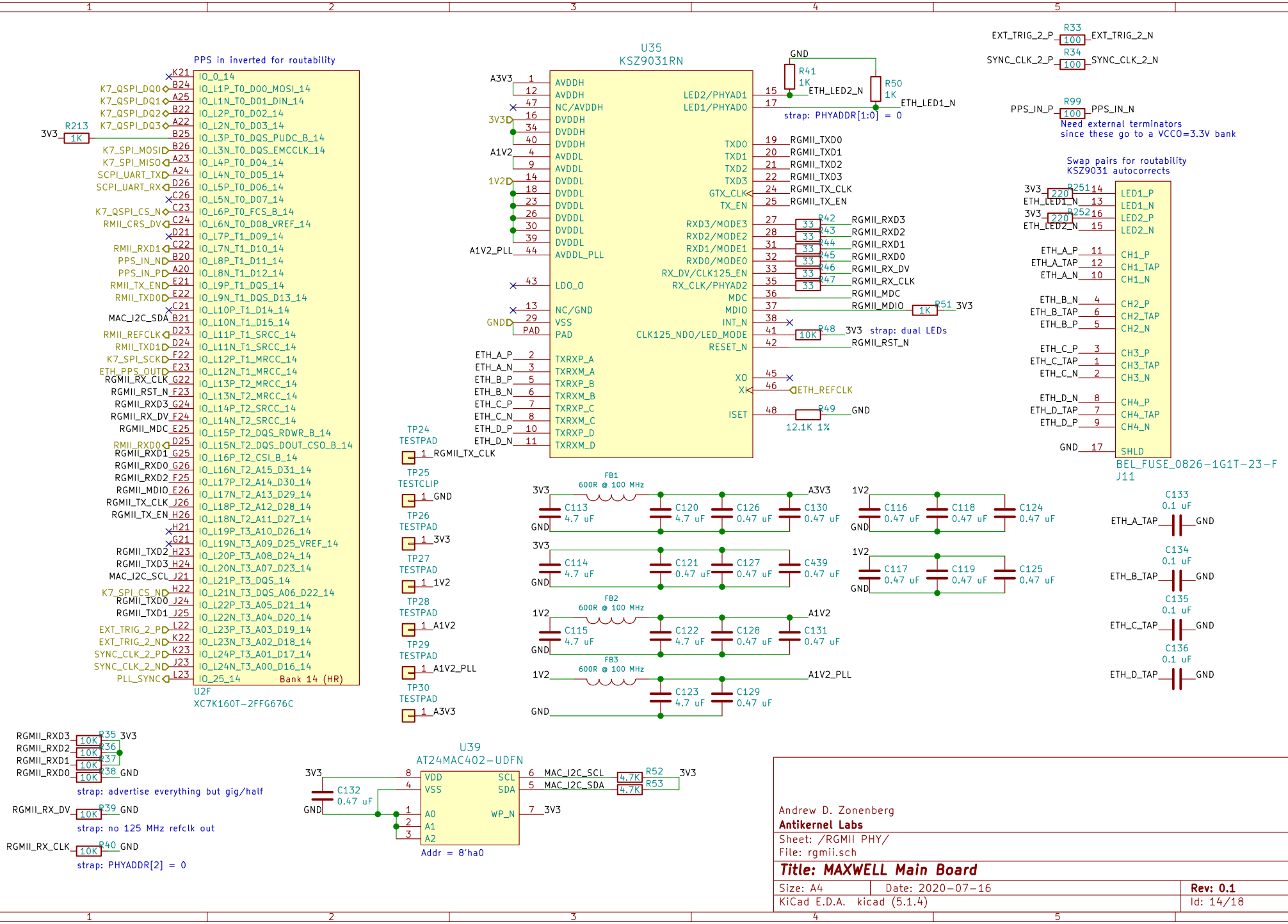
Sheet: /QSFP+/
File: qsfp.sch
Title: MAXWELL Main Board
Size: A4
Date: 2020-07-16
Rev: 0.1
KiCad E.D.A. kicad (5.1.4)
Id: 13/18


PPS in inverted for routability
U2F
XC7K160T-2FFG676C
Bank 14 (HR)
U35
KSZ9031RN
strap: PHYADDR[1:0] = 0
strap: dual LEDs
12.1K 1%
Need external terminators
since these go to a VCCO=3.3V bank
Swap pairs for routability
KSZ9031 autocorrects
BEL_FUSE_0826-1G1T-23-F
J11
FB1
FB2
FB3
600R @ 100 MHz
U39
AT24MAC402-UDFN
Addr = 8'ha0
strap: advertise everything but gig/half
strap: no 125 MHz refclk out
strap: PHYADDR[2] = 0
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Sheet: /RGMII PHY/
File: rgmii.sch
Title: MAXWELL Main Board
Size: A4
Date: 2020-07-16
Rev: 0.1
KiCad E.D.A. kicad (5.1.4)
Id: 14/18

Swap ext refclk polarity for routing
This just introduces a 180 deg phase shift
If we need ultra precise sync we can correct

U36A
LMK04806B

CLK_OCXO_AC_P 28 CLKIN0_P
CLK_OCXO_AC_N 29 CLKIN0_N
REF_IN_AC_N 25 CLKIN1_P
REF_IN_AC_P 26 CLKIN1_N
VCXO_AC_P 36 OSCIN_P
VCXO_AC_N 37 OSCIN_N

CLKOUT0_P 1 S7_CLK_P
CLKOUT0_N 2 S7_CLK_N
CLKOUT1_P 4 K7_CLK_P
CLKOUT1_N 3 K7_CLK_N
CLKOUT2_P 13 RAM_CLK_P
CLKOUT2_N 14 RAM_CLK_N
CLKOUT3_P 16 LA_REFCLK_P
CLKOUT3_N 15 LA_REFCLK_N
CLKOUT4_P 19 SYNC_CLK_1_P
CLKOUT4_N 20 SYNC_CLK_1_N
CLKOUT5_P 22 SYNC_CLK_2_P
CLKOUT5_N 21 SYNC_CLK_2_N
CLKOUT6_P 48 REF_OUT_P
CLKOUT6_N 49 REF_OUT_N
CLKOUT7_P 51 REF_OUT
CLKOUT7_N 50
CLKOUT8_P 53 XG_REFCLK_P
CLKOUT8_N 54 XG_REFCLK_N
CLKOUT9_P 56
CLKOUT9_N 55
CLKOUT10_P 58 ETH_REFCLK
CLKOUT10_N 59
CLKOUT11_P 61
CLKOUT11_N 60
OSCOUT0_P 39
OSCOUT0_N 40
OSCOUT1_P 31
OSCOUT1_N 32

156.25 MHz LVDS
100 MHz LVDS
TBD MHz LVDS
Reference output, default 10 MHz
156.25 MHz LVDS
25 MHz LVCMOS

U36B
LMK04806B

3V3 10 VCC1_VCO
VCC_CLK23 17 VCC2_CLK23
VCC_CLK45 18 VCC3_CLK45
3V3 24 VCC4_D
30 VCC5_CLKIN
VCC_PLL1 35 VCC6_PLL1_CP1
3V3 38 VCC7_PLL2
VCC_PLL2 41 VCC8_PLL2_CP2
3V3 43 VCC9_PLL2
VCC_CLK67 47 VCC10_CLKOUT67
VCC_CLK89 52 VCC11_CLKOUT89
VCC_CLK67 57 VCC12_CLKOUT1011
VCC_CLK89 64 VCC13_CLKOUT02
GNDD 23 GND
PAD GND

LDObyp1 11
LDObyp2 12
CPOUT1 34 VCP1
CPOUT2 42 VCP2

C229 0.1 uF
C230 10 uF
GND

U36C
LMK04806B

PLL_SYNC 6 SYNC
PLL_SPI_LE 44 UWIRE_LE
PLL_SPI_CLK 45 UWIRE_CLK
PLL_SPI_DATA 46 UWIRE_DATA
PLL_STATUS_HOLDOVER 27 STATUS_HOLDOVER
PLL_STATUS_LD 33 STATUS_LD
PLL_STATUS_CLKIN0 62 STATUS_CLKIN0
PLL_STATUS_CLKIN1 63 STATUS_CLKIN1

R244 10K 3V3

U46
AOCJYR-10.000MHZ-M5625LF

3V3 C281 10 uF GND
1 NC
3V3 4 Vdd
GND 2 Vss
CLK 3
R76 33
C409 0.1 uF
CLK_OCXO_AC 11

U38B
LMH7322

5V0 14 VCCI
5V0_N 15 VSS
VCCO 18 2V5
VCCO 21
IN_P 12
IN_N GND
Q_P 20 CLK_OCXO_P
Q_N 19 CLK_OCXO_N
RHREF 10
R83 4.99K
RHYS 13
LE_P 17
R92 10K 5V0_N
LE_N 16
R131 10K 2V5

GND R84 62 CLK_OCXO_P
R89 62 CLK_OCXO_N
R132 240 2V5
R139 240

5V0 C416 4.7 uF GND
5V0_N C419 4.7 uF
2V5 C421 4.7 uF

3V3 C410 4.7 uF GND
C411 0.47 uF
C412 0.47 uF
C413 0.47 uF

FB4 600R @ 100 MHz
3V3 C286 4.7 uF GND
VCC_CLK23 C289 0.47 uF
FB7 600R @ 100 MHz
3V3 VCC_PLL1 C294 0.47 uF GND
FB6 600R @ 100 MHz
3V3 VCC_CLK45 C291 0.47 uF GND

FB9 600R @ 100 MHz
3V3 VCC_CLK67 C296 0.47 uF GND C414 0.47 uF
FB5 600R @ 100 MHz
3V3 VCC_CLK89 C290 0.47 uF GND C415 0.47 uF
FB8 600R @ 100 MHz
3V3 VCC_PLL2 C295 0.47 uF GND

C231 0.1 uF
CLK_OCXO_P CLK_OCXO_AC_P
R94 100
CLK_OCXO_N CLK_OCXO_AC_N
C232 0.1 uF

C233 0.1 uF
REF_IN_P REF_IN_AC_P
R95 100
REF_IN_N REF_IN_AC_N
C234 0.1 uF

Termination and AC coupling for clock inputs

U47
565BAA100M000ABG

3V3 C418 0.47 uF GND
6 VDD
3 GND
OUT_P 4 VCXO_N
OUT_N 5 VCXO_P
VCP1 1 CTL
3V3 2 EN

VCP1
C284 5.6 nF
C287 270 nF
R140 3.9K
GND

VCP2
C285 39 pF
C288 3.3 nF
R141 820
GND

PLL configuration

PLL1_R = 1
PLL1_N = 1
PLL1 PFD freq = 10 MHz
PLL1 VCXO: 100 MHz
VCO tune slope = 60 ppm/V = 6 kHz/V
PLL1 CP = 1.6 mA
PLL1 loop filter:
* R2 = 3.9K
* C1 = 5.6 nF
* C2 = 270 nF
OSCout_DIV = 1

PLL2_R = 2
PLL2_N_PRE = 2
PLL2_N = 25
PLL2 PFD = 50 MHz
PLL2 CP = 3.2 mA
PLL2 loop filter:
* C1 = 39 pF
* C2 = 3.3 nF
* C3 = 0.01 nF (integrated)
* C4 = 0.01 nF (integrated)
* R2 = 820
* R3 = 200 (integrated)
* R4 = 200 (integrated)

PLL2 VCO = 2.5 GHz

C292 0.1 uF
VCXO_P VCXO_AC_P
R238 100
VCXO_N VCXO_AC_N
C293 0.1 uF

Flip polarity of VCXO output for routability
This introduces a constant 180 deg phase shift,
which the PLL won't care about.

GND C101 0.1 uF
2V5 7 VCC
VT0 2
VT1 3 1V2
1V2 8 VCCO
13 VCCO
EQ 6 TRIG_OUT_MUX_EQ
GND 14 PAD
GND
GND
TRIG_OUT_SEL 15 SEL
TRIG_OUT_P 16 IN0_P
TRIG_OUT_N 1 IN0_N
Q_P 11 TRIG_OUT_MUX_P
Q_N 10 TRIG_OUT_MUX_N
R150 49.9 GND
GTX_TRIG_OUT_P 4 IN1_P
GTX_TRIG_OUT_N 5 IN1_N
SY56017R
U45

2V5 C97 0.1 uF C98 0.01 uF GND
1V2 C102 0.1 uF C103 0.01 uF C104 0.1 uF C105 0.01 uF

TP31 TESTCLIP 1 3V3
TP32 TESTCLIP 1 GND
TP33 TESTPAD 1 VCC_CLK23
TP34 TESTPAD 1 VCC_PLL1
TP35 TESTPAD 1 VCC_CLK45
TP36 TESTPAD 1 VCC_CLK67
TP37 TESTPAD 1 VCC_CLK89
TP38 TESTPAD 1 VCC_PLL2
TP39 TESTCLIP 1 GND

TP40 TESTCLIP 1 PLL_STATUS_HOLDOVER
TP41 TESTCLIP 1 PLL_STATUS_LD
TP42 TESTCLIP 1 PLL_STATUS_CLKIN0
TP43 TESTCLIP 1 PLL_STATUS_CLKIN1
TP44 TESTPAD 1 CLK_OCXO_AC

Sheet: Trigger and Reference Inputs
EXT_TRIG_1_P TRIG_IN_1_P
EXT_TRIG_1_N TRIG_IN_1_N
EXT_TRIG_2_P TRIG_IN_2_P
EXT_TRIG_2_N TRIG_IN_2_N
REF_IN_P REF_IN_P
REF_IN_N REF_IN_N
PPS_IN_P PPS_IN_P
PPS_IN_N PPS_IN_N
REF_OUT_P REF_OUT_P
REF_OUT_N REF_OUT_N
REF_OUT REF_OUT
TRIG_OUT_MUX_P TRIG_OUT
5V0 5V0
2V5 2V5
GND GND
5V0_N 5V0_N
File: trigger.sch

TRIG_OUT_MUX is one leg of a 1.2V CML output
DC coupled, 390 mV swing or −4 dBm

REF_OUT is single ended LVCMOS33
-3.3V swing or +14 dBm

REF_OUT_P/N is LVDS, 400 mV or −4 dBm

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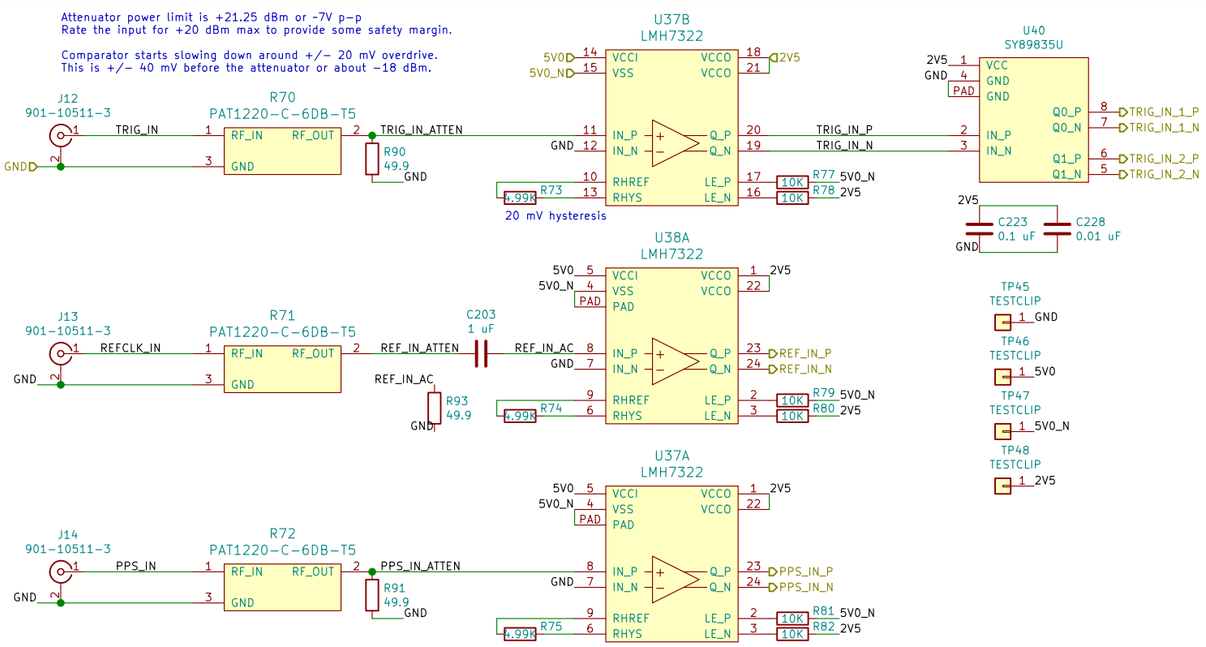
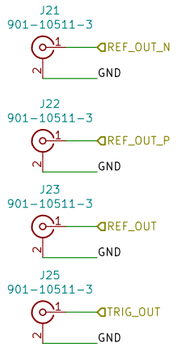
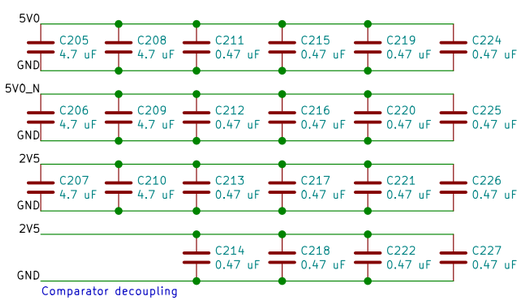
Antikernel Labs
Sheet: /Clocking/
File: clocking.sch
Title: MAXWELL Main Board
Size: A3 | Date: 2020-07-16 | **Rev: 0.1**
KiCad E.D.A. kicad (5.1.4) | Id: 15/18

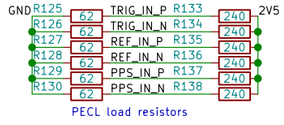
Attenuator power limit is +21.25 dBm or ~7V p-p
Rate the input for +20 dBm max to provide some safety margin.

Comparator starts slowing down around +/- 20 mV overdrive.
This is +/- 40 mV before the attenuator or about -18 dBm.









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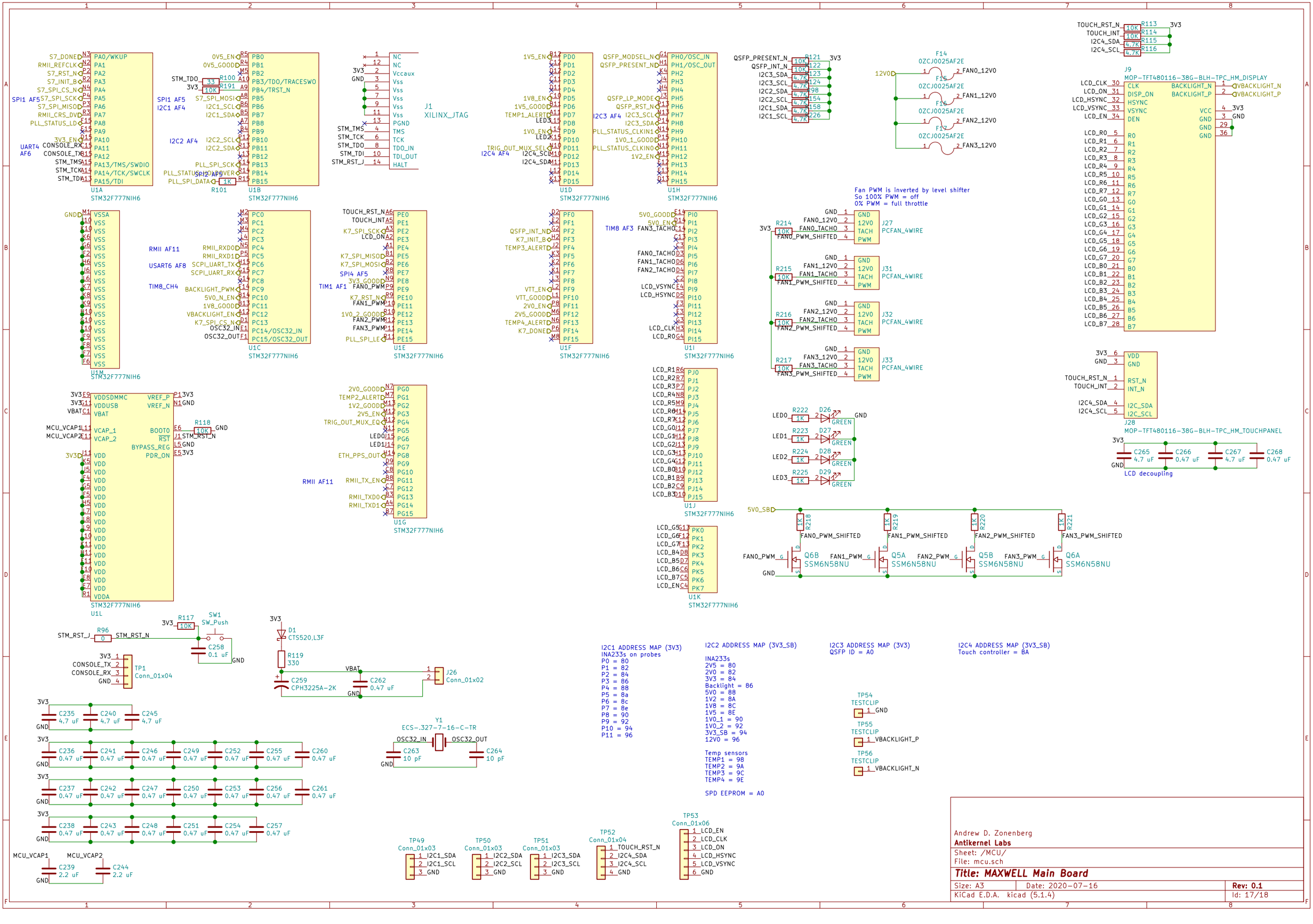
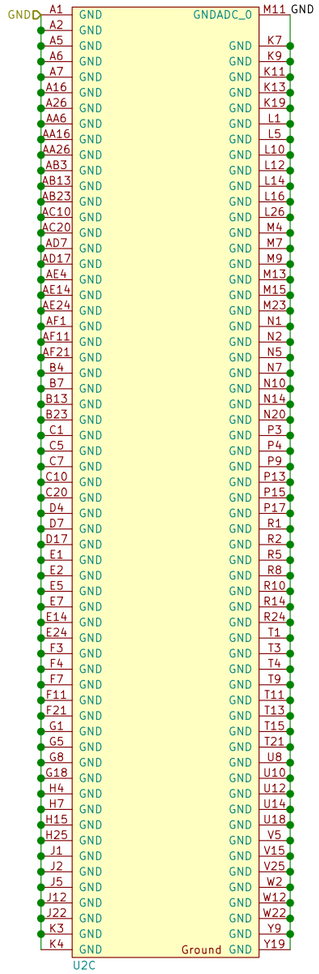
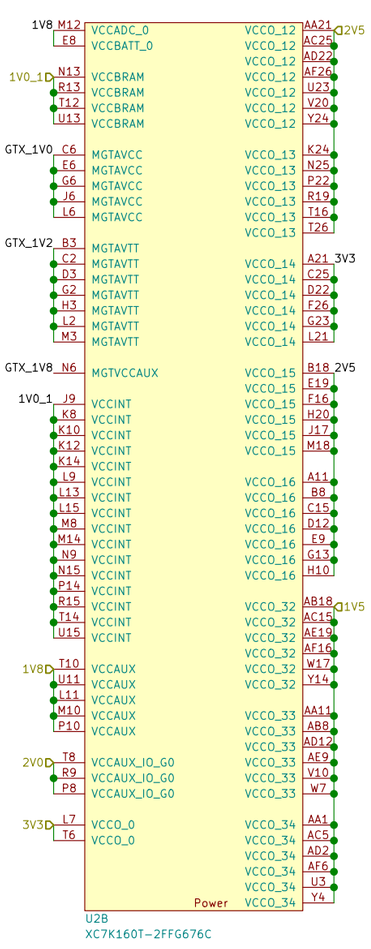
Sheet: /Clocking/Trigger and Reference Inputs/
File: trigger.sch

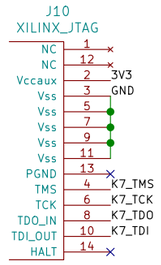
Title: MAXWELL Main Board

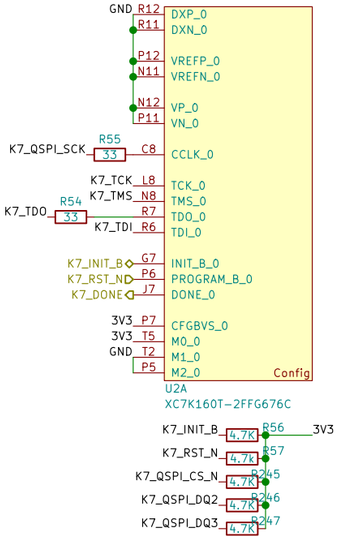
Size: A3	Date: 2020-07-16	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.4)		Id: 16/18

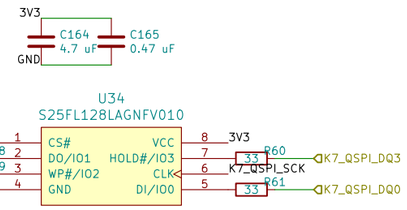

U1A
STM32F777NIH6
PA0/WKUP
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13/TMS/SWDIO
PA14/TCK/SWCLK
PA15/TDI
S7_DONE
RMII_REFCLK
S7_RST_N
S7_INIT_B
S7_SPI_CS_N
S7_SPI_SCK
S7_SPI_MISO
RMII_CRS_DV
PLL_STATUS_LD
3V3_EN
CONSOLE_RX
CONSOLE_TX
STM_TMS
STM_TCK
STM_TDI
SPI1 AF5
UART4 AF6
U1B
PB0
PB1
PB2
PB3/TDO/TRACESWO
PB4/TRST_N
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
0V5_EN
0V5_GOODD
STM_TDO
3V3
S7_SPI_MOSI
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
PLL_SPI_SCK
PLL_STATUS_OVER
PLL_SPI_DATA
SPI2 AF5
I2C1 AF4
I2C2 AF4
R101
1K
R100
33
R191
10K
J1
XILINX_JTAG
NC
Vccaux
Vss
PGND
TMS
TCK
TDO_IN
TDI_OUT
HALT
STM_TMS
STM_TCK
STM_TDO
STM_TDI
STM_RST_J
U1D
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PD8
PD9
PD10
PD11
PD12
PD13
PD14
PD15
1V5_EN
1V8_EN
1V5_GOODD
TEMP1_ALERTD
LED3
1V0_EN
LED2
TRIG_OUT_MUX_SEL
I2C4_SCL
I2C4_SDA
I2C4 AF4
U1H
PH0/OSC_IN
PH1/OSC_OUT
PH2
PH3
PH4
PH5
PH6
PH7
PH8
PH9
PH10
PH11
PH12
PH13
PH14
PH15
QSFP_MODSEL_N
QSFP_PRESENT_N
QSFP_LP_MODE
QSFP_RST_N
I2C3_SCL
I2C3_SDA
PLL_STATUS_CLKIN1
1V0_1_GOODD
PLL_STATUS_CLKIN0
1V2_EN
I2C3 AF4
QSFP_PRESENT_N
QSFP_INT_N
I2C3_SCL
I2C3_SDA
I2C2_SDA
I2C2_SCL
I2C1_SDA
I2C1_SCL
R121
10K
122
4.7K
123
4.7K
124
4.7K
98
4.7K
154
4.7K
158
4.7K
226
4.7K
3V3
F14
0ZCJ0025AF2E
F15
F16
F17
12V0
FAN0_12V0
FAN1_12V0
FAN2_12V0
FAN3_12V0
U1M
STM32F777NIH6
VSSA
VSS
GNDD
U1C
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
PC12
PC13
PC14/OSC32_IN
PC15/OSC32_OUT
RMII AF11
USART6 AF8
TIM8_CH4
RMII_RXD0D
RMII_RXD1D
SCPI_UART_TX
SCPI_UART_RX
BACKLIGHT_PWM
5V0_N_EN
1V8_GOODD
VBACKLIGHT_EN
K7_SPI_CS_N
OSC32_IN
OSC32_OUT
U1E
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PE8
PE9
PE10
PE11
PE12
PE13
PE14
PE15
TOUCH_RST_N
TOUCH_INT
K7_SPI_SCK
LCD_ON
K7_SPI_MISO
K7_SPI_MOSI
SPI4 AF5
3V3_GOODD
TIM1 AF1
FAN0_PWM
K7_RST_N
FAN1_PWM
1V0_2_GOODD
FAN2_PWM
FAN3_PWM
PLL_SPI_LE
U1F
PF0
PF1
PF2
PF3
PF4
PF5
PF6
PF7
PF8
PF9
PF10
PF11
PF12
PF13
PF14
PF15
QSFP_INT_N
K7_INIT_B
TEMP3_ALERT
VTT_EN
VTT_GOODD
2V0_EN
2V5_GOODD
TEMP4_ALERT
K7_DONE
U1I
PI0
PI1
PI2
PI3
PI4
PI5
PI6
PI7
PI8
PI9
PI10
PI11
PI12
PI13
PI14
PI15
5V0_GOODD
5V0_EN
TIM8 AF3
FAN3_TACHO
FAN0_TACHO
FAN1_TACHO
FAN2_TACHO
LCD_VSYNC
LCD_HSYNC
LCD_CLK
LCD_RO
U1J
PJ0
PJ1
PJ2
PJ3
PJ4
PJ5
PJ6
PJ7
PJ8
PJ9
PJ10
PJ11
PJ12
PJ13
PJ14
PJ15
LCD_R1
LCD_R2
LCD_R3
LCD_R4
LCD_R5
LCD_R6
LCD_R7
LCD_G0
LCD_G1
LCD_G2
LCD_G3
LCD_B0
LCD_B1
LCD_B2
LCD_B3
U1K
PK0
PK1
PK2
PK3
PK4
PK5
PK6
PK7
LCD_G5
LCD_G6
LCD_G7
LCD_B4
LCD_B5
LCD_B6
LCD_B7
LCD_EN
U1G
PG0
PG1
PG2
PG3
PG4
PG5
PG6
PG7
PG8
PG9
PG10
PG11
PG12
PG13
PG14
PG15
2V0_GOODD
TEMP2_ALERTD
1V2_GOODD
2V5_EN
TRIG_OUT_MUX_EQ
LED0
LED1
ETH_PPS_OUT
RMII_TX_EN
RMII_TXD0
RMII_TXD1
U1L
VDDSDMMC
VDDUSB
VBAT
VCAP_1
VCAP_2
BOOT0
BYPASS_REG
PDR_ON
VDD
VDDA
VREF_P
VREF_N
RST
3V3
GND
MCU_VCAP1
MCU_VCAP2
R118
10K
STM_RST_N
R96
0
R117
10K
SW1
SW_Push
C258
0.1 uF
TP1
Conn_01x04
CONSOLE_TX
CONSOLE_RX
D1
CTS520,L3F
R119
330
C259
CPH3225A-2K
C262
0.47 uF
J26
Conn_01x02
VBAT
C235
C240
C245
4.7 uF
C236
C241
C246
C249
C252
C255
C260
0.47 uF
C237
C242
C247
C250
C253
C256
C261
C238
C243
C248
C251
C254
C257
C239
C244
2.2 uF
Y1
ECS-.327-7-16-C-TR
OSC32_IN
OSC32_OUT
C263
C264
10 pF
TP49
TP50
TP51
TP52
TP53
Conn_01x03
Conn_01x04
Conn_01x06
I2C1_SDA
I2C1_SCL
I2C2_SDA
I2C2_SCL
I2C3_SDA
I2C3_SCL
TOUCH_RST_N
I2C4_SDA
I2C4_SCL
LCD_EN
LCD_CLK
LCD_ON
LCD_HSYNC
LCD_VSYNC
I2C1 ADDRESS MAP (3V3)
INA233s on probes
P0 = 80
P1 = 82
P2 = 84
P3 = 86
P4 = 88
P5 = 8a
P6 = 8c
P7 = 8e
P8 = 90
P9 = 92
P10 = 94
P11 = 96
I2C2 ADDRESS MAP (3V3_SB)
INA233s
2V5 = 80
2V0 = 82
3V3 = 84
Backlight = 86
5V0 = 88
1V2 = 8A
1V8 = 8C
1V5 = 8E
1V0_1 = 90
1V0_2 = 92
3V3_SB = 94
12V0 = 96
Temp sensors
TEMP1 = 98
TEMP2 = 9A
TEMP3 = 9C
TEMP4 = 9E
SPD EEPROM = A0
I2C3 ADDRESS MAP (3V3)
QSFP ID = A0
I2C4 ADDRESS MAP (3V3_SB)
Touch controller = BA
Fan PWM is inverted by level shifter
So 100% PWM = off
0% PWM = full throttle
R214
10K
FAN0_TACHO
FAN0_PWM_SHIFTED
J27
PCFAN_4WIRE
R215
FAN1_TACHO
FAN1_PWM_SHIFTED
J31
R216
FAN2_TACHO
FAN2_PWM_SHIFTED
J32
R217
FAN3_TACHO
FAN3_PWM_SHIFTED
J33
GND
12V0
TACH
PWM
LED0
LED1
LED2
LED3
R222
R223
R224
R225
1K
D26
D27
D28
D29
GREEN
5V0_SB
R218
R219
R220
R221
Q6B
Q5A
Q5B
Q6A
SSM6N58NU
J9
MOP-TFT480116-38G-BLH-TPC_HM_DISPLAY
CLK
DISP_ON
HSYNC
VSYNC
DEN
RO
R1
R2
R3
R4
R5
R6
R7
G0
G1
G2
G3
G4
G5
G6
G7
B0
B1
B2
B3
B4
B5
B6
B7
BACKLIGHT_N
BACKLIGHT_P
VCC
VBACKLIGHT_N
VBACKLIGHT_P
J28
MOP-TFT480116-38G-BLH-TPC_HM_TOUCHPANEL
RST_N
INT_N
I2C_SDA
I2C_SCL
C265
C266
C267
C268
4.7 uF
0.47 uF
LCD decoupling
TP54
TP55
TP56
TESTCLIP
VBACKLIGHT_P
VBACKLIGHT_N
Andrew D. Zonenberg
Antikernel Labs
Sheet: /MCU/
File: mcu.sch
Title: MAXWELL Main Board
Size: A3
Date: 2020-07-16
Rev: 0.1
KiCad E.D.A. kicad (5.1.4)
Id: 17/18

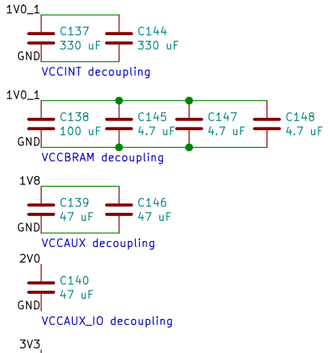


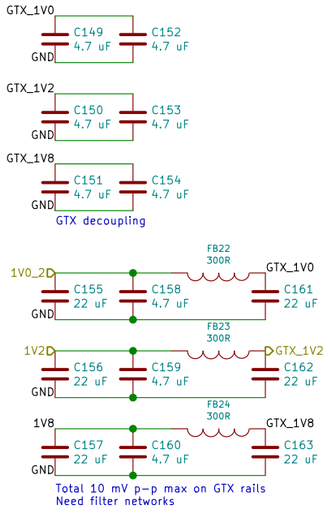


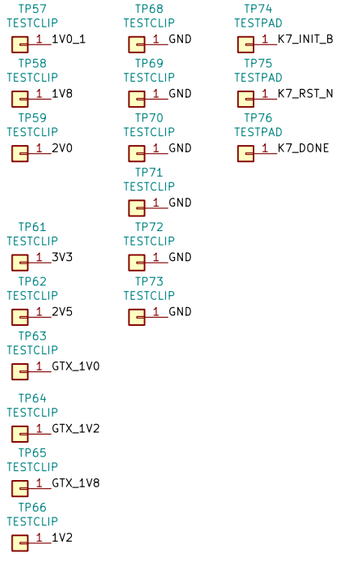












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Sheet: /FPGA Support/
File: fpgasupport.sch

Title: MAXWELL Main Board

Size: A3	Date: 2020-07-16	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.4)		Id: 18/18