J1 SMA
1 VIN
2 GND
MAX −2V to +2V INPUT

R1 PS3216GT2−R50−T1
IN OUT0
GND OUT1
GND_4 VIN_0 VIN_1 LTRIG_VT

Level triggering
LTRIG_DIN LTRIG_VT
3V3_CLKBUF 3V3 1V8 GND 3V0_N
LTRIG_CDROUT_P LTRIG_CDROUT_N
LTRIG_SAMPOUT_P LTRIG_SAMPOUT_N
leveltrigger.sch

ADC
ADC_VT 3V3 1V8 GND 3V0_N
ADC_DIN ADC_VT 3V3 1V8 GND 3V0_N
ADC_OUT_P ADC_OUT_N ADC_LE_P ADC_LE_N
adc.sch

Power supply
12V0 D3V3 GND
A5V0 5V25 3V3 3V3_CLKBUF 3V3_PLL 2V5 1V8 1V0 3V0_N 3V3_N 5V0_N
psu.sch

CDR
PLL_CDRCLK_P PLL_CDRCLK_N
3V3_PLL 1V8 1V0 GND
OSC_PWR_EN OSC_OE OSC_OS OSC_FS1 OSC_FS0
SERDES_POWER_EN SERDES_MODE_SEL SERDES_RST_N SERDES_MDC SERDES_MDIO
CDR_EXTCLK_N CDR_EXTCLK_P
cdr.sch

External reference clocks
3V3 3V3_CLKBUF 1V8 GND 3V0_N
CDR_EXTCLK_P CDR_EXTCLK_N PLL_EXTCLK_P PLL_EXTCLK_N
REFCLK_SINGLE_VT EXT_CLK_SEL
SAMPLE_EXTCLK_P SAMPLE_EXTCLK_N
ext−clocks.sch

PLL
CDRCLK_P CDRCLK_N
OSC_PWR_EN OSC_OE OSC_OS OSC_FS1 OSC_FS0
3V3_PLL GND PLL_SYNC PLL_HOLDOVER PLL_LD PLL_LE PLL_CLK PLL_DATA PLL_CLKIN0 PLL_CLKIN1
3V3 GND SYNC STATUS_HOLDOVER STATUS_LD UWIRE_LE UWIRE_CLK UWIRE_DATA STATUS_CLKIN0 STATUS_CLKIN1
EXTCLK_P EXTCLK_N
SAMPCLK_P SAMPCLK_N
FPGACLK_P FPGACLK_N
pll.sch

Sample clock muxing
PLL_SAMPCLK_P PLL_SAMPCLK_N
SAMP_MUXSEL0 SAMP_MUXSEL1
3V3_CLKBUF GND
3V3 GND
SAMPLE_MUXSEL0 SAMPLE_MUXSEL1
EXT_SAMPCLK_P EXT_SAMPCLK_N
LVL_SAMPCLK_P LVL_SAMPCLK_N
CLKOUT1_N CLKOUT1_P CLKOUT0_N CLKOUT0_P
sample−clockmux.sch

J2 BARREL
1 2 3
12V0_RAW GND
F1 3A
FB1 MPZ2012S101AT000
12V0

M1 TRACEPAD
M2 LOGO1
M3 LOGO2
M4 LOGO3
M5 LOGO4
M6 LOGO5
M7 LOGO6
FID1 FIDUCIAL
FID2 FIDUCIAL
FID3 FIDUCIAL
FID4 FIDUCIAL
FID5 FIDUCIAL
FID6 FIDUCIAL

DAC
A5V0 1V8 GND 5V0_N
REFCLK_SINGLE_VT ADC_VT LTRIG_VT DAC_MUXOUT LDAC_N DAC_CS_N DAC_SCK DAC_MOSI DAC_MISO DAC_RST_N
dac.sch

One−Shot
ONESHOT_RST_P ONESHOT_RST_N
ADC_LE_P ADC_LE_N
3V3_CLKBUF 2V5 1V8 GND
CLKOUT_P CLKOUT_N
ONESHOT_FINEPHASE_P ONESHOT_FINEPHASE_N
ONESHOT_COARSEPHASE_P ONESHOT_COARSEPHASE_N
ONESHOT_TRIGGERED_P ONESHOT_TRIGGERED_N
TRIGGERED_P TRIGGERED_N
RANGE_SEL
oneshot.sch

J11 SMA
J12 SMA
GND
Phase shifted sampling clock out
for debugging or external logic

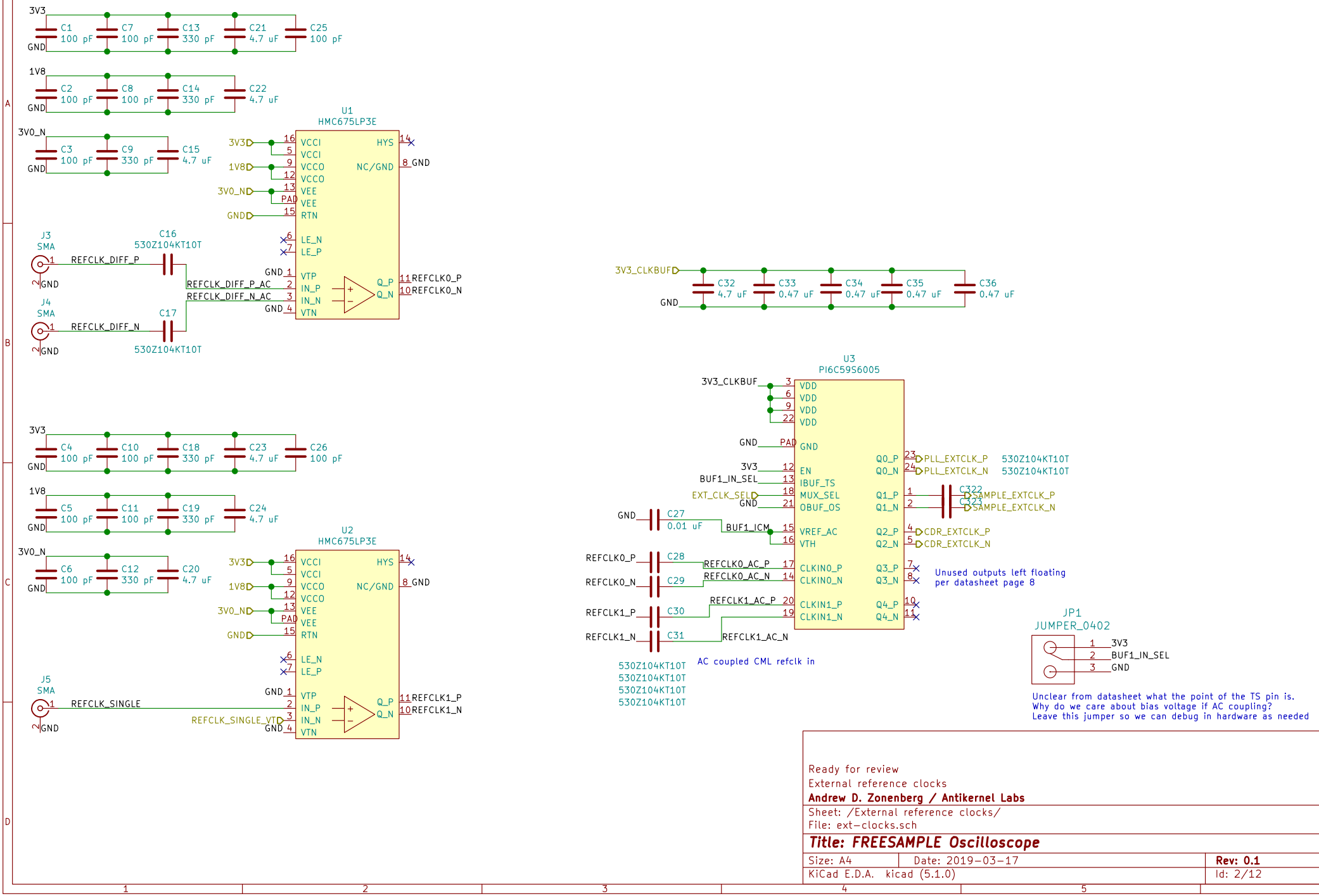
Phase control
FINEPHASE_P FINEPHASE_N
COARSEPHASE_P COARSEPHASE_N
3V3 GND 3V3_N
COARSE_EN COARSE_SLOAD COARSE_SDIN COARSE_SCLK
FINE_SEL0_P FINE_SEL0_N
FINE_SEL1_P FINE_SEL1_N
FINE_SEL2_P FINE_SEL2_N
FINE_SEL3_P FINE_SEL3_N
FINE_SEL4_P FINE_SEL4_N
CLKIN0_P CLKIN0_N CLKIN1_P CLKIN1_N
phase−control.sch

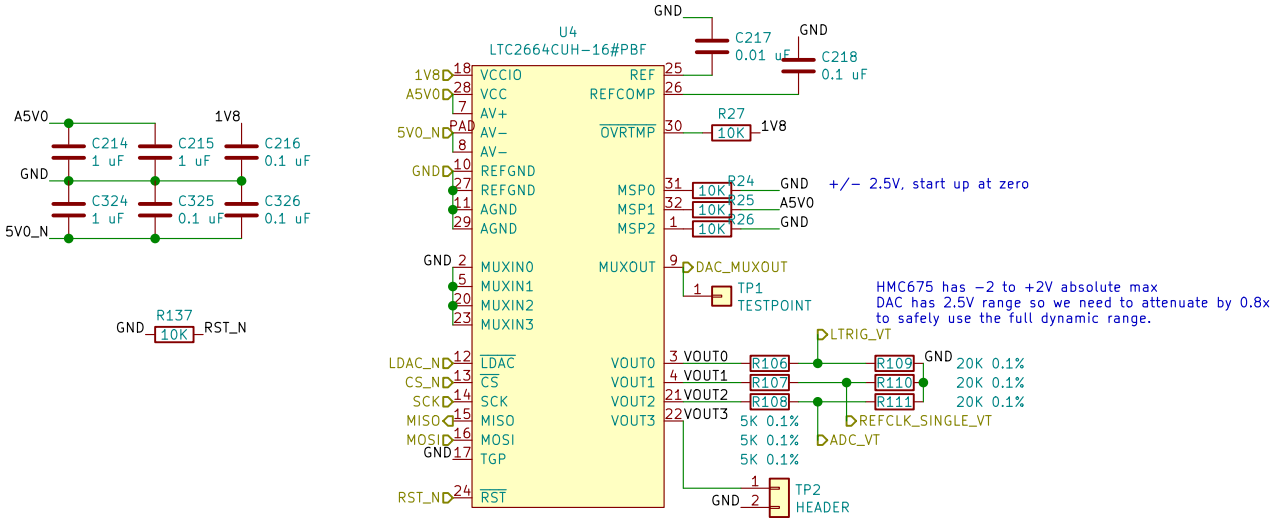
SoM connectors
LVCMOS33
5V25 D3V3 GND D2V5 D1V8
EXT_CLK_SEL OSC_OE OSC_OS OSC_FS1 OSC_FS0 PLL_SYNC PLL_HOLDOVER PLL_LD PLL_LE PLL_CLK PLL_DATA PLL_CLKIN0 PLL_CLKIN1 SAMP_MUXSEL0 SAMP_MUXSEL1 RANGE_SEL COARSE_EN COARSE_SLOAD COARSE_SDIN COARSE_SCLK OSC_PWR_EN
LVDS
FPGA_CLK_P FPGA_CLK_N FINE_SEL_0_PD FINE_SEL_0_ND FINE_SEL_1_PD FINE_SEL_1_ND FINE_SEL_2_PD FINE_SEL_2_ND FINE_SEL_3_PD FINE_SEL_3_ND FINE_SEL_4_PD FINE_SEL_4_ND ONESHOT_RST_PD ONESHOT_RST_ND TRIGGERED_PD TRIGGERED_ND ADC_OUT_PD ADC_OUT_ND
FPGACLK_P FPGACLK_N FINE_SEL0_P FINE_SEL0_N FINE_SEL1_P FINE_SEL1_N FINE_SEL2_P FINE_SEL2_N FINE_SEL3_P FINE_SEL3_N FINE_SEL4_P FINE_SEL4_N ONESHOT_RST_P ONESHOT_RST_N TRIGGERED_P TRIGGERED_N ADC_OUT_P ADC_OUT_N
Analog sensors
DAC_MUXOUT
LVCMOS18
LDAC_ND DAC_CS_ND DAC_SCK DAC_MOSI DAC_MISO DAC_RST_ND SERDES_MODE_SEL SERDES_RST_ND SERDES_MDC SERDES_MDIO SERDES_POWER_END
LDAC_N DAC_CS_N DAC_SCK DAC_MOSI DAC_MISO DAC_RST_N SERDES_MODE_SEL SERDES_RST_N SERDES_MDC SERDES_MDIO SERDES_POWER_EN
som.sch

Ready for review
Top Level
**Andrew D. Zonenberg / Antikernel Labs**

| | |
|---|---|
| Sheet: / | |
| File: freesample.sch | |
| ***Title: FREESAMPLE Oscilloscope*** | |
| Size: A3 | Date: 2019−03−17 |
| KiCad E.D.A. kicad (5.1.0) | Id: 1/12 |

**Rev: 0.1**


3V3
C1 100 pF
C7 100 pF
C13 330 pF
C21 4.7 uF
C25 100 pF
GND
1V8
C2 100 pF
C8 100 pF
C14 330 pF
C22 4.7 uF
3V0_N
C3 100 pF
C9 330 pF
C15 4.7 uF
U1
HMC675LP3E
VCCI
VCCO
VEE
RTN
LE_N
LE_P
VTP
IN_P
IN_N
VTN
HYS
NC/GND
PAD
Q_P
Q_N
J3
SMA
C16
530Z104KT10T
REFCLK_DIFF_P
REFCLK_DIFF_P_AC
J4
SMA
C17
530Z104KT10T
REFCLK_DIFF_N
REFCLK_DIFF_N_AC
REFCLK0_P
REFCLK0_N
3V3_CLKBUF
C32 4.7 uF
C33 0.47 uF
C34 0.47 uF
C35 0.47 uF
C36 0.47 uF
U3
PI6C59S6005
VDD
EN
IBUF_TS
MUX_SEL
OBUF_OS
VREF_AC
VTH
CLKIN0_P
CLKIN0_N
CLKIN1_P
CLKIN1_N
Q0_P
Q0_N
Q1_P
Q1_N
Q2_P
Q2_N
Q3_P
Q3_N
Q4_P
Q4_N
BUF1_IN_SEL
EXT_CLK_SEL
BUF1_ICM
C27 0.01 uF
C28
C29
C30
C31
530Z104KT10T
530Z104KT10T
530Z104KT10T
530Z104KT10T
AC coupled CML refclk in
PLL_EXTCLK_P
PLL_EXTCLK_N
530Z104KT10T
530Z104KT10T
C322
C323
SAMPLE_EXTCLK_P
SAMPLE_EXTCLK_N
CDR_EXTCLK_P
CDR_EXTCLK_N
Unused outputs left floating
per datasheet page 8
JP1
JUMPER_0402
3V3
BUF1_IN_SEL
GND
Unclear from datasheet what the point of the TS pin is.
Why do we care about bias voltage if AC coupling?
Leave this jumper so we can debug in hardware as needed
C4 100 pF
C10 100 pF
C18 330 pF
C23 4.7 uF
C26 100 pF
C5 100 pF
C11 100 pF
C19 330 pF
C24 4.7 uF
C6 100 pF
C12 330 pF
C20 4.7 uF
U2
HMC675LP3E
J5
SMA
REFCLK_SINGLE
REFCLK_SINGLE_VT
REFCLK1_P
REFCLK1_N
Ready for review
External reference clocks
Andrew D. Zonenberg / Antikernel Labs
Sheet: /External reference clocks/
File: ext-clocks.sch
Title: FREESAMPLE Oscilloscope
Size: A4
Date: 2019-03-17
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)
Id: 2/12

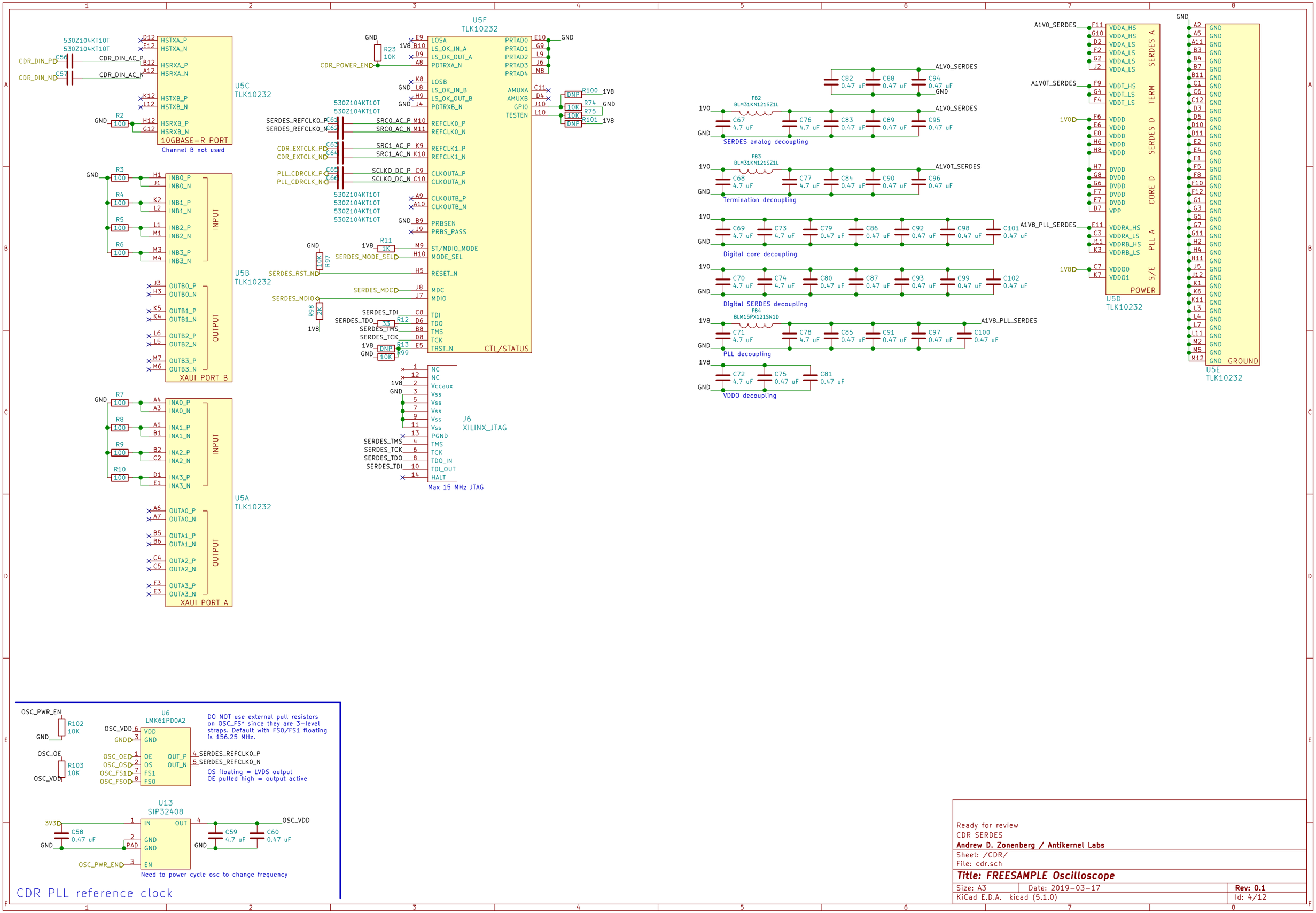


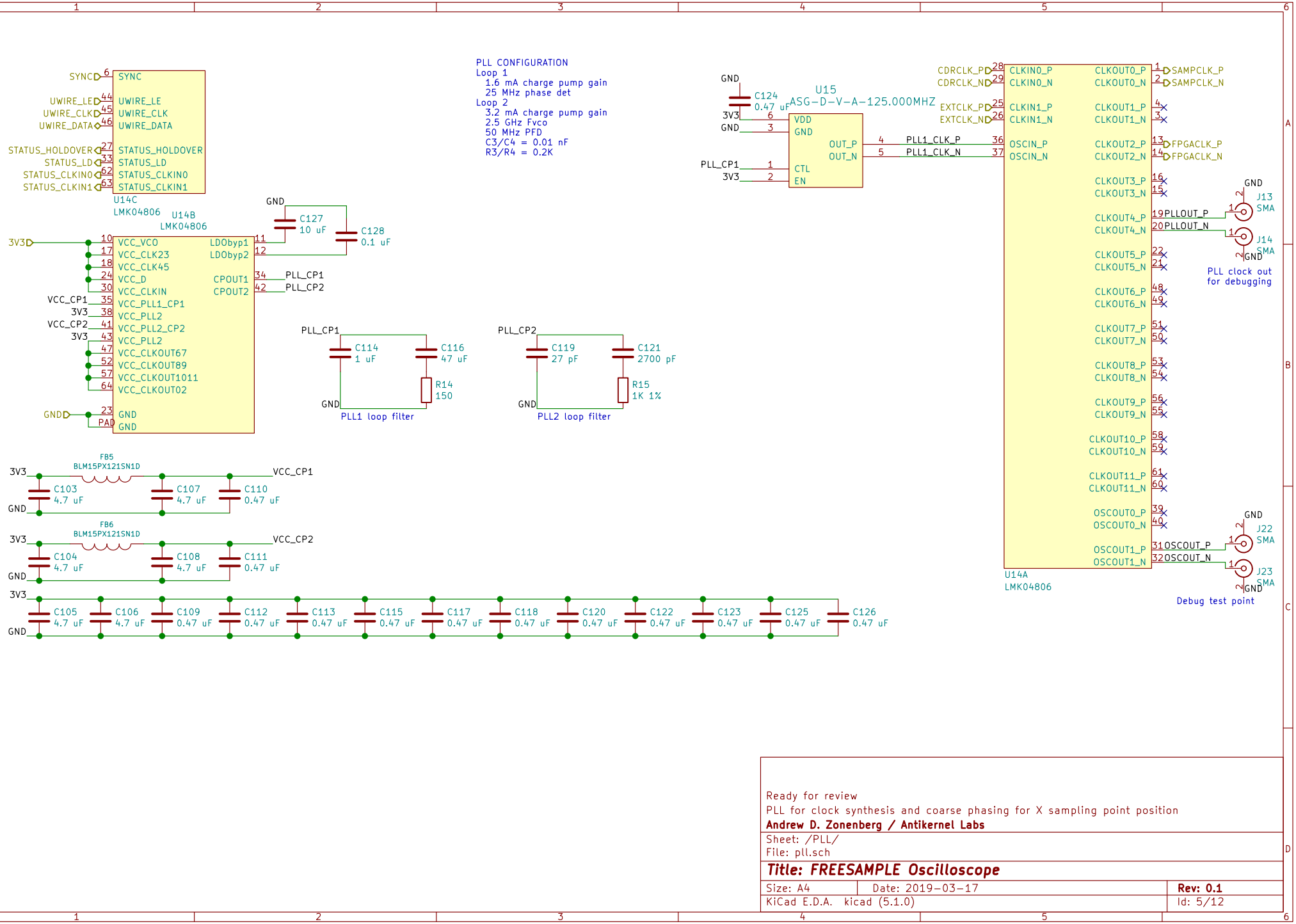

Ready for review
DAC for setting sampling point Y position
**Andrew D. Zonenberg / Antikernel Labs**

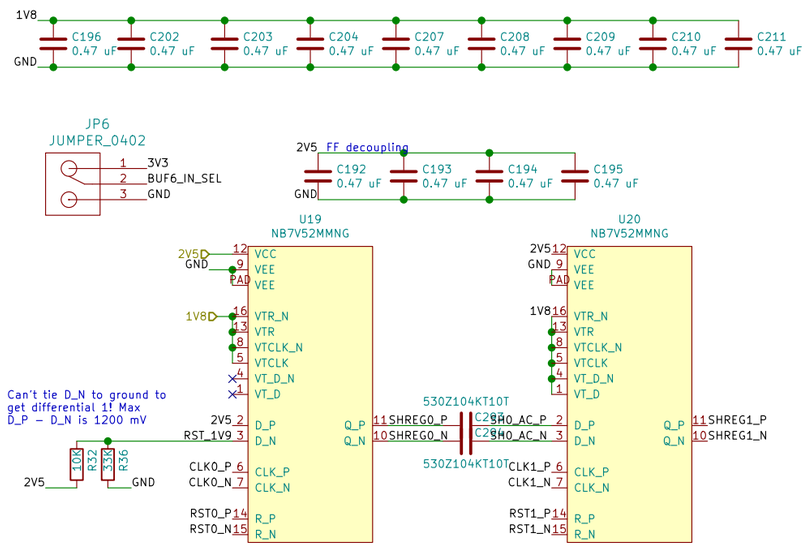
Sheet: /DAC/
File: dac.sch

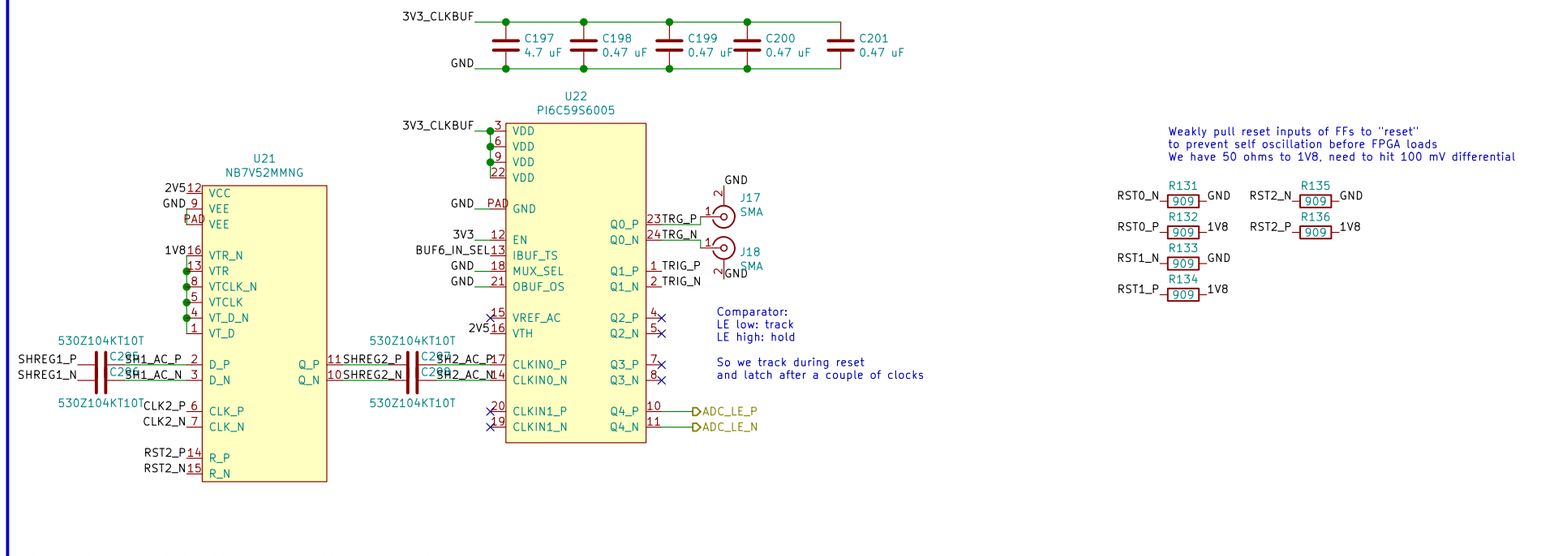
***Title: FREESAMPLE Oscilloscope***

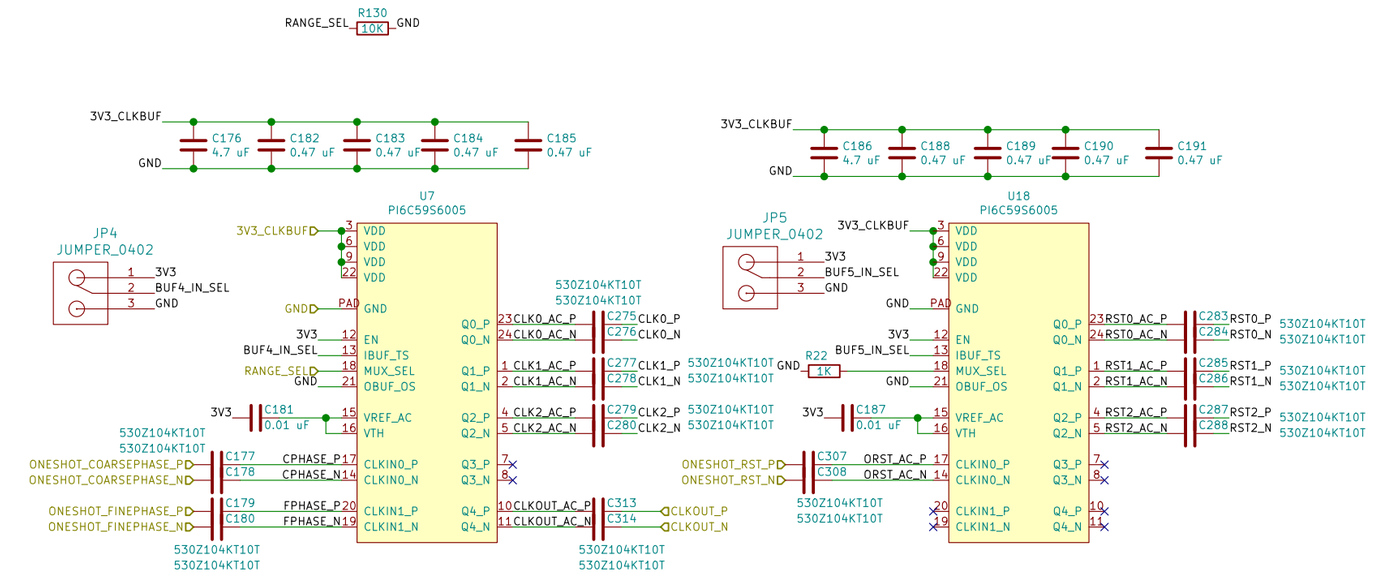
| Size: A4 | Date: 2019-03-17 | **Rev: 0.1** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.0) | | Id: 3/12 |

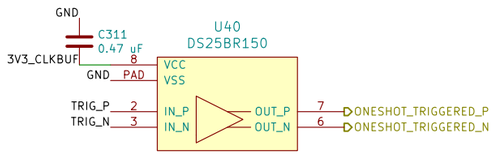

U5C
TLK10232
10GBASE-R PORT
Channel B not used
530Z104KT10T
530Z104KT10T
CDR_DIN_P
CDR_DIN_N
CDR_DIN_AC_P
CDR_DIN_AC_N
HSTXA_P
HSTXA_N
HSRXA_P
HSRXA_N
HSTXB_P
HSTXB_N
HSRXB_P
HSRXB_N
U5B
TLK10232
XAUI PORT B
INPUT
OUTPUT
INB0_P
INB0_N
INB1_P
INB1_N
INB2_P
INB2_N
INB3_P
INB3_N
OUTB0_P
OUTB0_N
OUTB1_P
OUTB1_N
OUTB2_P
OUTB2_N
OUTB3_P
OUTB3_N
U5A
TLK10232
XAUI PORT A
INA0_P
INA0_N
INA1_P
INA1_N
INA2_P
INA2_N
INA3_P
INA3_N
OUTA0_P
OUTA0_N
OUTA1_P
OUTA1_N
OUTA2_P
OUTA2_N
OUTA3_P
OUTA3_N
U5F
TLK10232
CTL/STATUS
LOSA
LS_OK_IN_A
LS_OK_OUT_A
PDTRXA_N
LOSB
LS_OK_IN_B
LS_OK_OUT_B
PDTRXB_N
REFCLK0_P
REFCLK0_N
REFCLK1_P
REFCLK1_N
CLKOUTA_P
CLKOUTA_N
CLKOUTB_P
CLKOUTB_N
PRBSEN
PRBS_PASS
ST/MDIO_MODE
MODE_SEL
RESET_N
MDC
MDIO
TDI
TDO
TMS
TCK
TRST_N
PRTAD0
PRTAD1
PRTAD2
PRTAD3
PRTAD4
AMUXA
AMUXB
GPIO
TESTEN
SRC0_AC_P
SRC0_AC_N
SRC1_AC_P
SRC1_AC_N
SCLKO_DC_P
SCLKO_DC_N
SERDES_REFCLK0_P
SERDES_REFCLK0_N
CDR_EXTCLK_P
CDR_EXTCLK_N
PLL_CDRCLK_P
PLL_CDRCLK_N
SERDES_MODE_SEL
SERDES_RST_N
SERDES_MDC
SERDES_MDIO
SERDES_TDI
SERDES_TDO
SERDES_TMS
SERDES_TCK
CDR_POWER_END
J6
XILINX_JTAG
Max 15 MHz JTAG
NC
Vccaux
Vss
PGND
TMS
TCK
TDO_IN
TDI_OUT
HALT
U5E
TLK10232
GROUND
U5D
TLK10232
POWER
SERDES A
SERDES D TERM
CORE D
PLL A
S/E
VDDA_HS
VDDA_LS
VDDT_HS
VDDT_LS
VDDD
VDDR_HS
VDDR_LS
VDDO0
VDDO1
VPP
A1V0_SERDES
A1V0T_SERDES
A1V8_PLL_SERDES
SERDES analog decoupling
Termination decoupling
Digital core decoupling
Digital SERDES decoupling
PLL decoupling
VDDO decoupling
FB2
FB3
FB4
BLM31KN121SZ1L
BLM15PX121SN1D
U6
LMK61PD0A2
DO NOT use external pull resistors on OSC_FS* since they are 3-level straps. Default with FS0/FS1 floating is 156.25 MHz.
OS floating = LVDS output
OE pulled high = output active
U13
SIP32408
Need to power cycle osc to change frequency
CDR PLL reference clock
Ready for review
CDR SERDES
Andrew D. Zonenberg / Antikernel Labs
Sheet: /CDR/
File: cdr.sch
Title: FREESAMPLE Oscilloscope
Size: A3
Date: 2019-03-17
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)
Id: 4/12


PLL CONFIGURATION
Loop 1
1.6 mA charge pump gain
25 MHz phase det
Loop 2
3.2 mA charge pump gain
2.5 GHz Fvco
50 MHz PFD
C3/C4 = 0.01 nF
R3/R4 = 0.2K
U14C
LMK04806
U14B
LMK04806
U15
ASG-D-V-A-125.000MHZ
U14A
LMK04806
PLL1 loop filter
PLL2 loop filter
PLL clock out
for debugging
Debug test point
Ready for review
PLL for clock synthesis and coarse phasing for X sampling point position
Andrew D. Zonenberg / Antikernel Labs
Sheet: /PLL/
File: pll.sch
Title: FREESAMPLE Oscilloscope
Size: A4
Date: 2019-03-17
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)
Id: 5/12



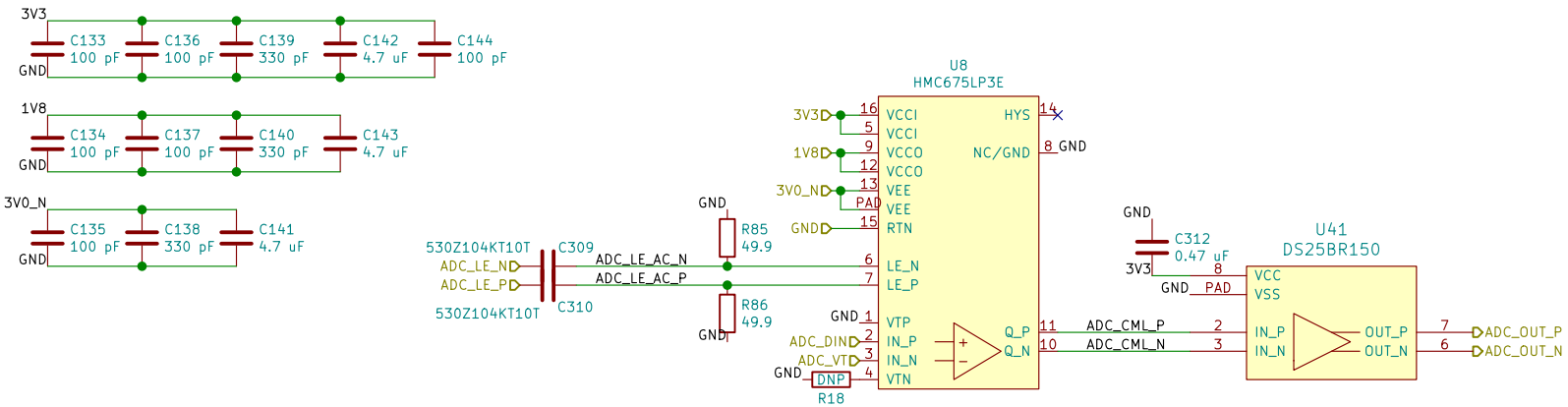




Ready for review
Trigger phase alignment from FPGA to recovered clock domain
**Andrew D. Zonenberg / Antikernel Labs**

Sheet: /One–Shot/
File: oneshot.sch

***Title: FREESAMPLE Oscilloscope***

| Size: A3 | Date: 2019–03–17 | **Rev: 0.1** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.0) | | Id: 6/12 |

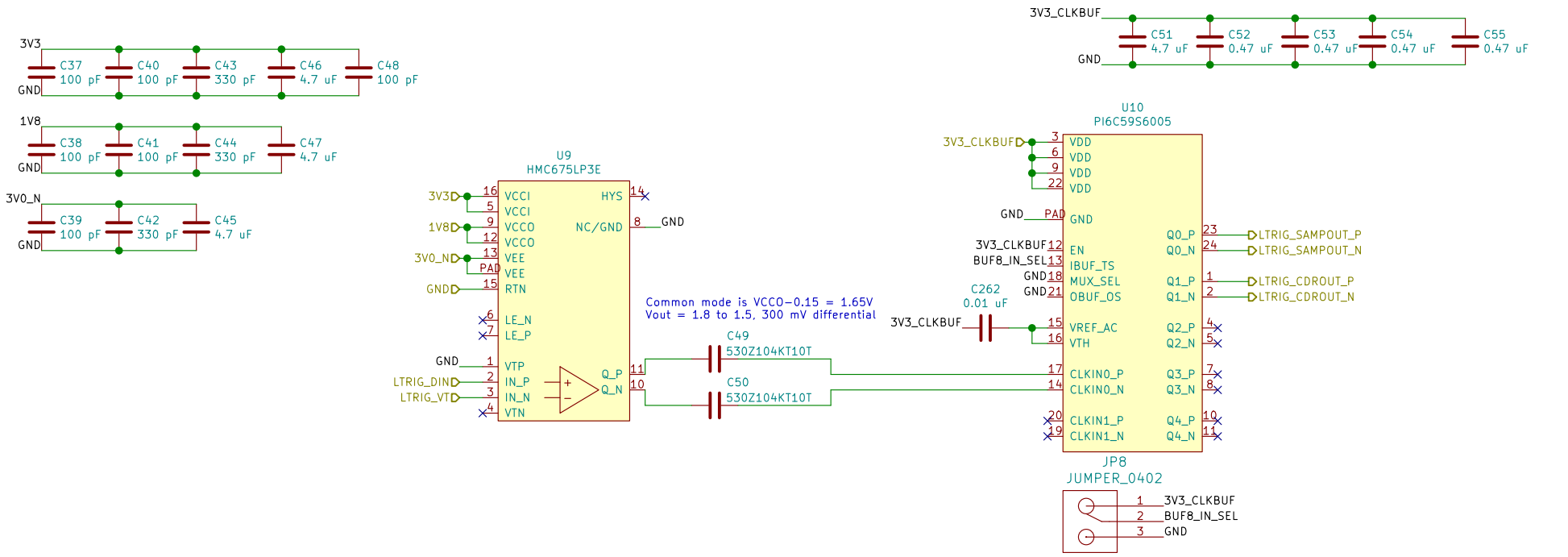



Ready for review
Ready for review
**Andrew D. Zonenberg / Antikernel Labs**

Sheet: /ADC/
File: adc.sch

***Title: FREESAMPLE Oscilloscope***

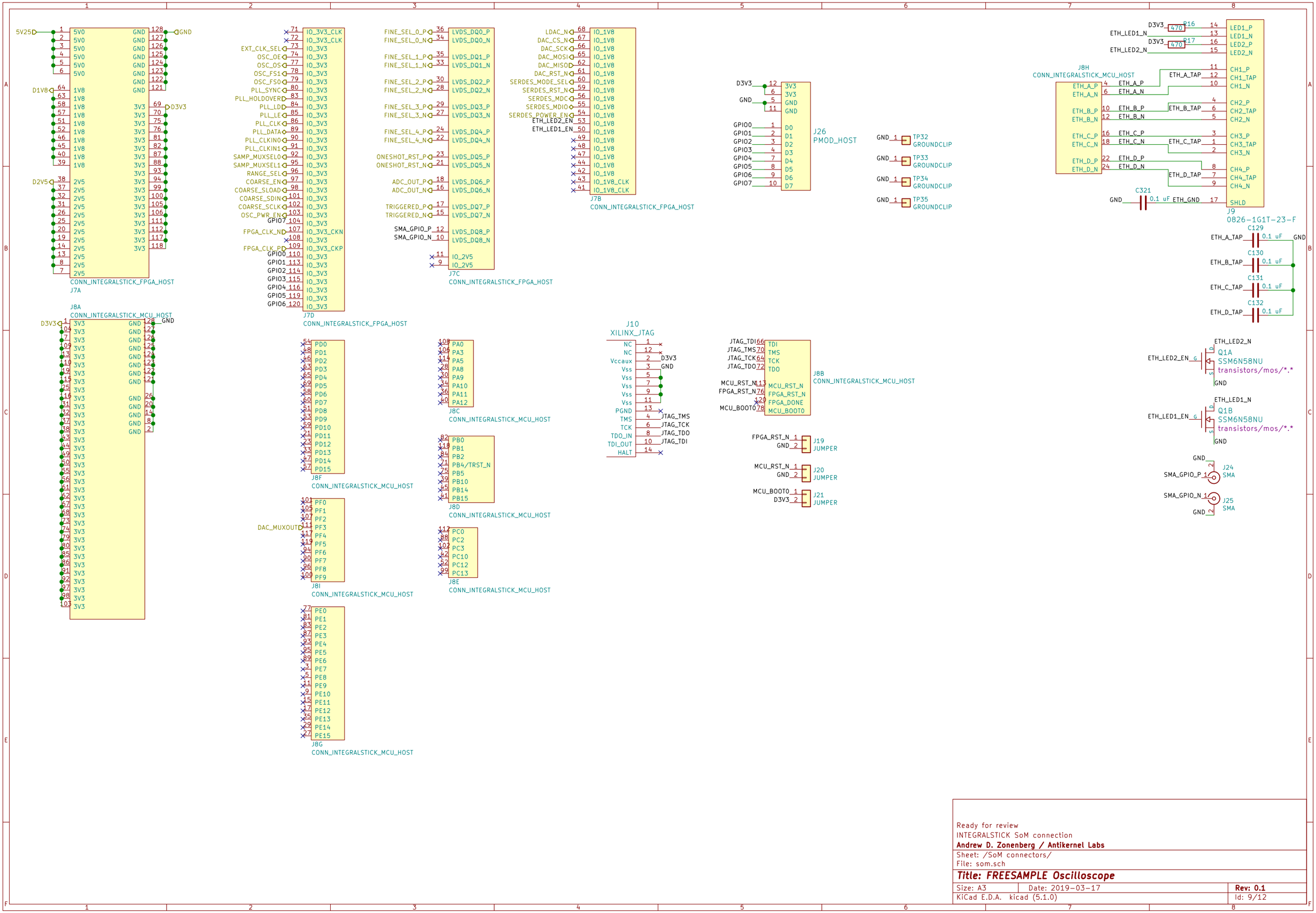
| Size: A4 | Date: 2019-03-17 | **Rev: 0.1** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.0) | | Id: 7/12 |

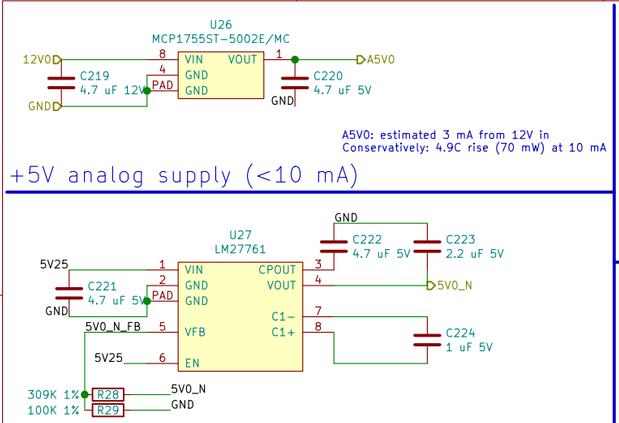


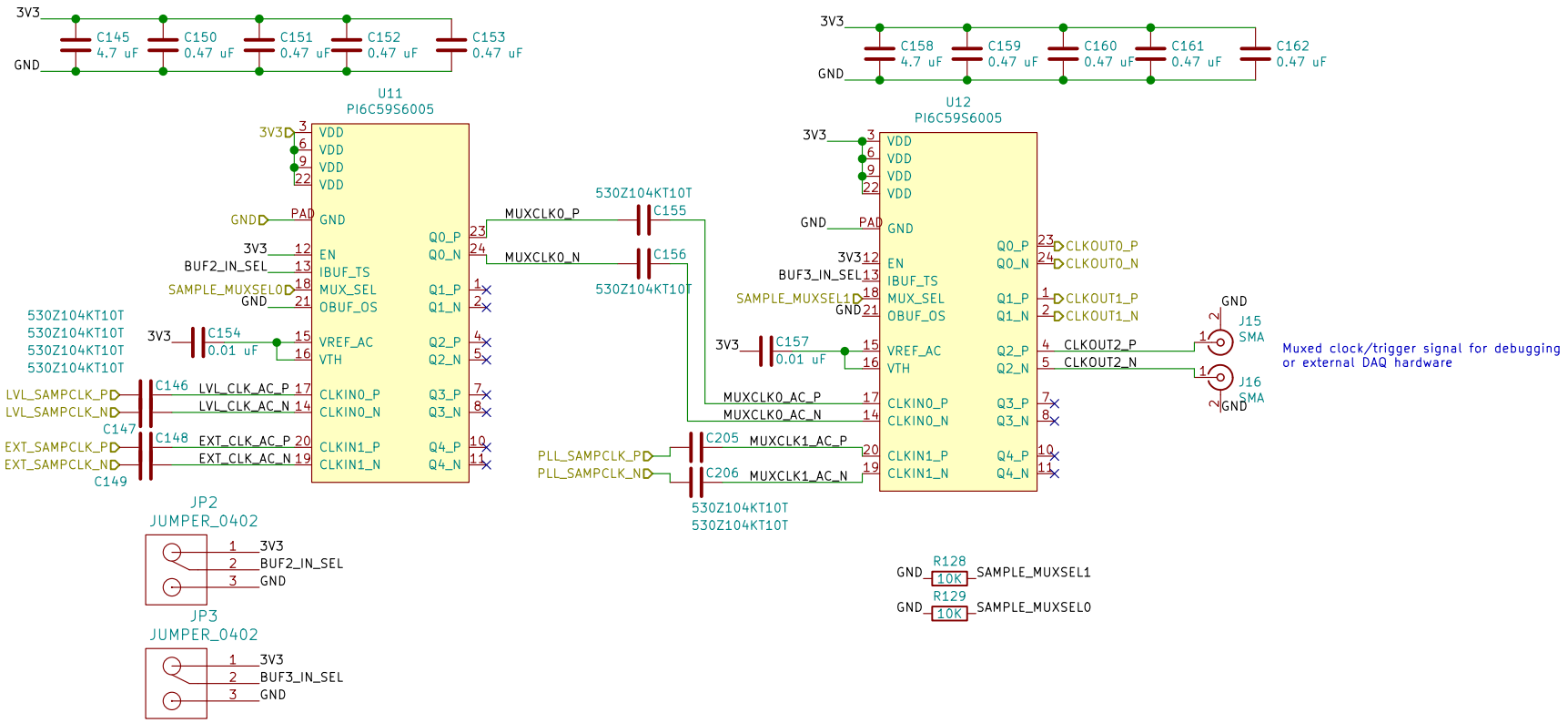

Ready for review
Level triggering
**Andrew D. Zonenberg / Antikernel Labs**
Sheet: /Level triggering/
File: leveltrigger.sch

***Title: FREESAMPLE Oscilloscope***

| Size: A4 | Date: 2019-03-17 | **Rev: 0.1** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.0) | | Id: 8/12 |


5V25
D1V8
D2V5
D3V3
GND
CONN_INTEGRALSTICK_FPGA_HOST
J7A
J8A
CONN_INTEGRALSTICK_MCU_HOST
J7D
J7C
J7B
J8C
J8F
J8D
J8I
J8E
J8G
J10
XILINX_JTAG
J26
PMOD_HOST
J8B
J19
JUMPER
J20
J21
TP32
TP33
TP34
TP35
GROUNDCLIP
J9
0826-1G1T-23-F
C321
C129
C130
C131
C132
0.1 uF
R16
R17
470
Q1A
Q1B
SSM6N58NU
transistors/mos/*.*
J24
J25
SMA
Ready for review
INTEGRALSTICK SoM connection
Andrew D. Zonenberg / Antikernel Labs
Sheet: /SoM connectors/
File: som.sch
Title: FREESAMPLE Oscilloscope
Size: A3
Date: 2019-03-17
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)
Id: 9/12


U26
MCP1755ST-5002E/MC
12V0
C219
4.7 uF 12V
C220
4.7 uF 5V
A5V0
GND
A5V0: estimated 3 mA from 12V in
Conservatively: 4.9C rise (70 mW) at 10 mA
+5V analog supply (<10 mA)
U27
LM27761
5V25
C221
4.7 uF 5V
C222
4.7 uF 5V
C223
2.2 uF 5V
5V0_N
C224
1 uF 5V
5V0_N_FB
309K 1%
100K 1%
R28
R29
5V0_N: estimated 3 mA from 5.25V in
Vout = −1.22 * (R28+R29)/R29
R29 > 50 kR (use 100K)
Use 309K (ideal 309.836K) for −4.99V
SMPS w/ 3 mA load, no thermal
analysis necessary
−5V analog supply (3 mA)
U30
OKL-T/3-W12P-C
R38
20K
C235
22 uF 16V
1V1_PGOOD
1V1_SENSE
R39
10K
R57
0
1V15_INT
C236
22 uF 10V
R37
10.5K
Rtrim(k) = 5.91 / (1.15 − 0.591) = 10.57K nominal
1.15V intermediate rail (2.6A)
U28
ADP1763Z-1.0
C225
4.7 uF
C228
22 uF
C229
1 uF
C226
1 uF
C227
22 nF
R33
5 mR
C233
22 uF
1V0
1V0_REF
1V0_SS
1V0_SENSE
1V0_VADJ
R31
0
R40
DNP
R30
1K
1V0_PGOOD
U29
ADP1763Z-1.0
C230
4.7 uF
C232
22 uF
C231
1 uF
R34
5 mR
C234
22 uF
R35
0
Vout = 3.0 * (Radj * 50 uA)
Radj = 1V/(150 uA) = 6.667 kR
Use 6.65K for 0.9975V
Connect two in parallel to spread out heat generation
0.15V * 3A = 0.45W total, estimate 0.3W worst case per chip
Assuming 1cm^2 plane for heatsinking, 30.8C rise.
Bigger planes will improve this
Typical SERDES power is << 3A which will also help,
especially if we power down the unused channel
1.0V CDR SERDES supply (2.6A)
U32
OKL-T/3-W12P-C
12V0
R42
20K
C240
22 uF 16V
5V0_PGOOD
5V0_SENSE
R46
10K
R47
0
D3V3
5V25
C243
22 uF 16V
R41
1.27K
Rtrim(k) = 5.91 / (5.25 − 0.591) = 1.27K
+5.25V supply for INTEGRALSTICK (<1A typ)
U31
ADP1741
3V5_INT2
C241
4.7 uF
C242
4.7 uF
3V3_CLKBUF
R43
0
3V3_CLKBUF_SENSE
R44
113K
R48
C239
10 nF
3V5_INT1
R45
20K 0.1%
100K
3V3_CLKBUF_PGOOD
0.2V drop * 2A = 0.4W
16.8C rise
Vout = 0.5*(1 + R44/R48), R48 < 60 kR
R44=113K gives 3.325V
+3.3V supply for clock buffers (1.4A)
U33
ADP1741
3V5_INT1
C246
4.7 uF
C248
4.7 uF
3V3_PLL
R49
0
3V3_PLL_SENSE
R51
113K
R55
C244
10 nF
R53
20K 1%
100K
3V3_PLL_PGOOD
0.2V drop * 0.85A = 0.17W
7.14C rise
+3.3V supply for PLL and VCO (0.85A)
U34
ADP1741
3V5_INT1
C247
4.7 uF
C249
4.7 uF
3V3
R50
0
3V3_SENSE
R52
113K
R56
C245
10 nF
R54
20K 1%
100K
3V3_PGOOD
0.2V drop * 0.25A = 0.05W
2.1C rise
+3.3V supply for other loads (0.25A)
U35
OKL-T/3-W12P-C
12V0
R59
20K
C237
22 uF 16V
3V5_PGOOD
3V5_SENSE
R60
10K
R61
0
3V5_INT1
C238
22 uF 10V
R58
2.05K
Rtrim(k) = 5.91 / (3.5 − 0.591) = 2.03K nominal
+3.5V intermediate rail 1 (1.4A)
U36
OKL-T/3-W12P-C
12V0
R63
20K
C250
22 uF 16V
3V5_PGOOD2
3V5_SENSE2
R64
10K
R65
0
3V5_INT2
C251
22 uF 10V
R62
2.05K
Rtrim(k) = 5.91 / (3.5 − 0.591) = 2.03K nominal
+3.5V intermediate rail 2 (1.4A)
U37
LM27761
3V5_INT1
C253
4.7 uF 5V
C254
4.7 uF 5V
C256
2.2 uF 5V
3V0_N
C257
1 uF 5V
3V0_N_FB
147K 1%
100K 1%
R66
R67
5V0_N
3V0_N: estimated 100 mA from 3.5V in
Vout = −1.22 * (R66+R67)/R67
R67 > 50 kR (use 100K)
Use 147k (ideal 145.9k) for −3.0V
Thermal analysis TODO
−3.0V supply for comparators (0.1A)
U39
LM27761
3V5_INT1
C258
4.7 uF 5V
C259
4.7 uF 5V
C260
2.2 uF 5V
3V3_N
C261
1 uF 5V
3V3_N_FB
174k 1%
100K 1%
R72
R73
5V0_N
3V3_N: estimated 100 mA from 3.5V in
Vout = −1.22 * (R66+R67)/R67
R67 > 50 kR (use 100K)
Use 174k (ideal 170.5k) for −3.3V
Thermal analysis TODO
−3.3V supply for delay line (0.2A)
U42
ADP1741
2V7_INT
C317
4.7 uF
C319
4.7 uF
2V5
R87
0
2V5_SENSE
R89
80.6K
R93
C315
10 nF
2V7_INT
R91
20K 1%
100K
2V5_PGOOD
0.2V drop * 0.5A = 0.1W
4.2C rise
+2.5V supply for flipflops (0.5A)
U43
ADP1741
2V7_INT
C318
4.7 uF
C320
4.7 uF
1V8
R88
0
1V8_SENSE
R90
52.3K
R94
C316
10 nF
2V7_INT
R92
20K 1%
100K
1V8_PGOOD
0.9V drop * 0.2A = 0.18W
7.6C rise
+1.8V supply for SERDES/comparators (0.2A)
U38
OKL-T/3-W12P-C
12V0
R69
20K
C252
22 uF 16V
2V7_PGOOD
2V7_SENSE
R70
10K
R71
0
2V7_INT
C255
22 uF 10V
R68
2.8K
Rtrim(k) = 5.91 / (2.7 − 0.591) = 2.80K nominal
+2.7V intermediate rail (0.7A)
A5V0
R112
953
GND
TP3
HEADER
5V0_N
R113
953
TP4
HEADER
Test points for low current power rails
Integrated 20x low−Z probes
1V15_INT
R114
453
TP5
1V0
R115
TP6
5V25
R116
TP7
3V3_CLKBUF
R117
TP8
3V3_PLL
R118
TP9
3V3
R119
TP10
3V5_INT1
R120
TP11
3V5_INT2
R121
TP12
3V0_N
R122
TP13
3V3_N
R123
TP14
2V5
R124
TP15
1V8
R125
TP16
2V7_INT
R126
TP17
12V0
R127
TP18
HEADER
Test points for power rails
Integrated 10x low−Z probes
GND
TP19
TESTCLIP
TP20
1V1_PGOOD
TP21
PROBEPAD
1V0_PGOOD
TP22
3V5_PGOOD
TP23
1V8_PGOOD
TP24
2V5_PGOOD
TP25
5V0_PGOOD
TP26
3V3_CLKBUF_PGOOD
TP27
3V3_PLL_PGOOD
TP28
3V3_PGOOD
TP29
3V5_PGOOD2
TP30
2V7_PGOOD
TP31
Test points for power−good signals
Ready for review
Ready for review
Andrew D. Zonenberg / Antikernel Labs
Sheet: /Power supply/
File: psu.sch
Title: FREESAMPLE Oscilloscope
Size: A3
Date: 2019-03-17
Rev: 0.1
KiCad E.D.A. kicad (5.1.0)
Id: 10/12




Ready for review
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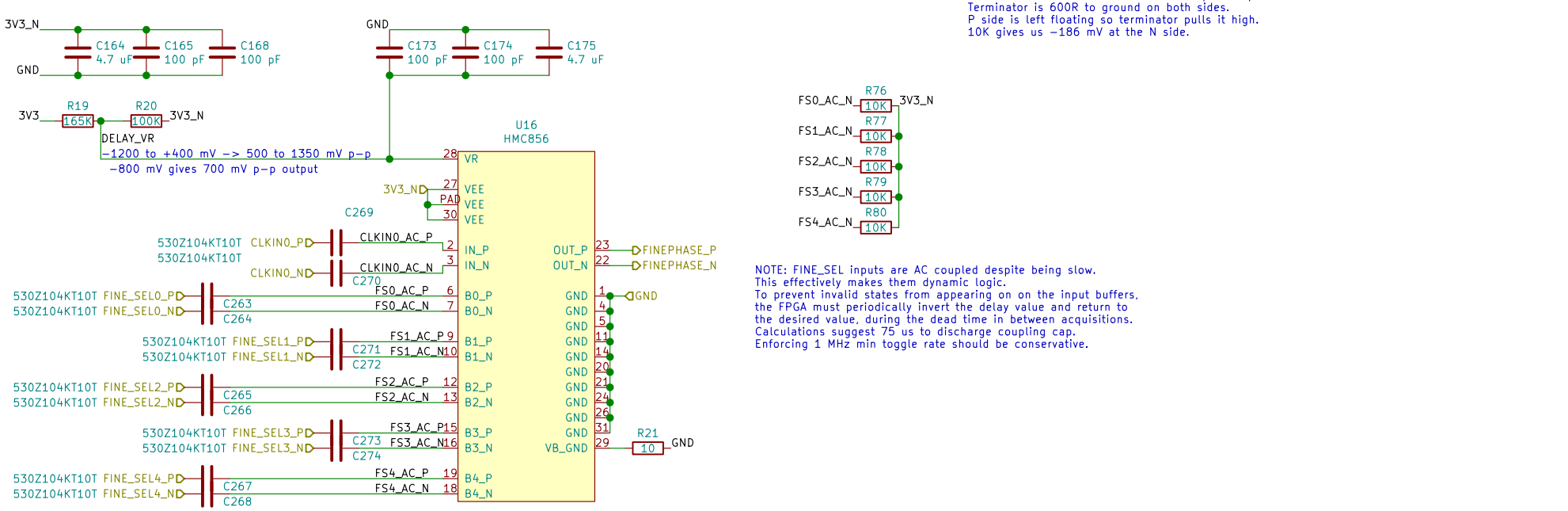
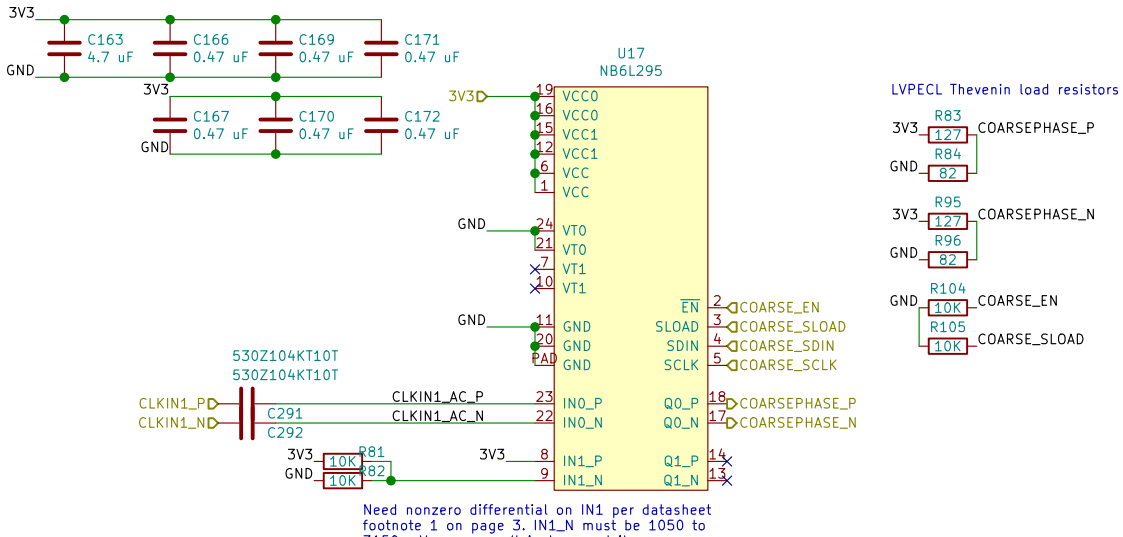
Sheet: /Sample clock muxing/
File: sample-clockmux.sch

***Title: FREESAMPLE Oscilloscope***

| Size: A4 | Date: 2019-03-17 | **Rev: 0.1** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.0) | | Id: 11/12 |




Fine delay line for PLL/CDR mode (1 Tsps max when combined w/ LMK04806)




Coarse delay line for non−repetitive triggers (90 GSa/s max)

Ready for review
Fine phase shifting for sampling point X position
**Andrew D. Zonenberg / Antikernel Labs**
Sheet: /Phase control/
File: phase−control.sch

***Title: FREESAMPLE Oscilloscope***

| Size: A4 | Date: 2019−03−17 | **Rev: 0.1** |
|---|---|---|
| KiCad E.D.A. kicad (5.1.0) | | Id: 12/12 |